Winbond Electronics Corp.

4M(512K × 8/256K × 16) SMARTVOLTAGE FLASH MEMORY

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1. GENERAL DESCRIPTION

The W28V400B/T Flash memory with SmartVoltage technology is a high-density, cost-effective, nonvolatile, read/write storage solution for a wide range of applications. It operates off of V_{DD} = 2.7V and V_{PP} = 2.7V. This low voltage operation capability realize battery life and suits for cellular phone application. Its Boot, Parameter and Main-blocked architecture, as well as low voltage and extended cycling. These features provide a highly flexible device suitable for portable terminals and personal computers. Additionally, the enhanced suspend capabilities provide an ideal solution for both code and data storage applications. For secure code storage applications, such as networking where code is either directly executed out of flash or downloaded to DRAM, the device offers four levels of protection. These are: absolute protection, enabled when $V_{PP} \leq V_{PPLK}$; selective hardware blocking; flexible software blocking; or write protection. These alternatives give designers comprehensive control over their code security needs. The device is manufactured on 0.35 μm process technology. It comes in industry-standard package: the 48-lead TSOP, ideal for board constrained applications.

2. FEATURES

- SmartVoltage Technology
  - V_{DD} = 2.7V, 3.3V or 5V
  - V_{PP} = 2.7V, 3.3V, 5V or 12V
- User-Configurable x 8 or x 16 Operation
- High-Performance Access Time
  - 85 nS (5V ±0.25V), 90 nS (5V ±0.5V), 100 nS (3.3V ±0.3V), 120 nS (2.7V to 3.6V)
- Operating Temperature
  - 0° C to +70° C
- Optimized Array Blocking Architecture
  - Two 4k-word (8k-byte) Boot Blocks
  - Six 4k-word (8k-byte) Parameter Blocks
  - Seven 32k-word (64k-byte) Main Blocks
  - Top Boot Location (W28V400TT)
  - Bottom Boot Location (W28V400BT)
- Extended Cycling Capability
  - Minimum 100,000 Block Erase Cycles
- Low Power Management
  - Deep Power-down Mode
  - Automatic Power Savings Mode Decreases I_{CCR} in Static Mode
- Enhanced Automated Suspend Options
  - Word/Byte Write Suspend to Read
  - Block Erase Suspend to Word/Byte Write
  - Block Erase Suspend to Read
- Enhanced Data Protection Features
  - Absolute Protection with $V_{PP} \leq V_{PPLK}$
  - Block Erase, Full Chip Erase, Word/Byte Write and Lock-Bit Configuration Lockout during Power Transitions
  - Block Blocks Protection with #WP = V_{IL}
- Automated Word/Byte Write and Block Erase
  - Command User Interface (CUI)
  - Status Register (SR)
- SRAM-Compatible Write Interface
- Industry-Standard Packaging
  - 48-Lead TSOP

3. PRODUCT OVERVIEW

The W28V400B/T is a high-performance 4M-bit SmartVoltage Flash memory organized as 512k-byte of 8 bits or 256k-word of 16 bits. The 512k-byte/256k-word of data is arranged in two 8k-byte/4k-word boot blocks, six 8k-byte/4k-word parameter blocks and seven 64kbyte/32k-word main blocks which are individually erasable in-system. The memory map is shown in Figure 3.

SmartVoltage technology provides a choice of V_{DD} and V_{PP} combinations, as shown in Table 1, to meet system performance and power expectations. 2.7V V_{DD} consumes approximately one-fifth the power of 5V V_{DD}. But, 5V V_{DD} provides the highest read performance. V_{PP} at 2.7, 3.3V and 5V eliminates the need for a separate 12V converter, while V_{PP} = 12V maximizes block erase and word/byte write performance. In addition to flexible erase and program voltages, the dedicated V_{PP} pin gives complete data protection when $V_{PP} \leq V_{PPLK}$.

Table 1. V_{DD} and V_{PP} Voltage Combinations Offered by SmartVoltage Technology

V_{DD} VOLTAGE	V_{PP} VOLTAGE
2.7V	2.7V, 3.3V, 5V, 12V
3.3V	3.3V, 5V, 12V
5V	5V, 12V

Internal V_{DD} and V_{PP} detection Circuitry automatically configures the device for optimized read and write operations.

A Command User Interface (CUI) serves as the interface between the system processor and internal operation of the device. A valid command sequence written to the CUI initiates device automation. An internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for block erase and word/byte write operations.

A block erase operation erases one of the device's 32k-word blocks typically within 0.39s (5V V_{DD}, 12V V_{PP}), 4k-word blocks typically within 0.25s (5V V_{DD}, 12V V_{PP}) independent of other blocks. Each block can be independently erased 100,000 times. Block erase suspend mode allows system software to suspend block erase to read or write data from any other block.

Writing memory data is performed in word/byte increments of the device's 32k-word blocks typically within 8.4 μS (5V V_{DD}, 12V VPP), 4k-word blocks typically within 17 μS (5V V_{DD}, 12V V_{PP}). Word/byte write suspend mode enables the system to read data or execute code from any other flash memory array location.

The boot blocks can be locked for the #WP pin. Block erase or word/byte write for boot block must not be carried out by #WP to Low and #RESET to V_{IH}.

The status register indicates when the WSM's block erase or word/byte write operation is finished.

The RY/#BY output gives an additional indicator of WSM activity by providing both a hardware signal of status (versus software polling) and status masking (interrupt masking for background block erase, for example). Status polling using RY/#BY minimizes both CPU overhead and system power consumption. When low, RY/#BY indicates that the WSM is performing a block erase or word/byte write. RY/#BY-high indicates that the WSM is ready for a new command, block erase is suspended (and word/byte write is inactive), word/byte write is suspended, or the device is in deep power-down mode.

The access time is 85ns (t_{AVQV}) over the commercial temperature range (0° C to +70° C) and V_{DD} supply voltage range of 4.75V to 5.25V. At lower V_{DD} voltages, the access times are 90ns (4.5V to 5.5V), 100 nS (3.0V to 3.6V) and 120 nS (2.7V to 3.6V).

The Automatic Power Savings (APS) feature substantially reduces active current when the device is in static mode (addresses not switching). In APS mode, the typical I_{CCR} current is 1mA at V_{DD} = 5V.

When #CE and #RESET pins are at V_{DD}, the I_{CC} CMOS standby mode is enabled. When the #RESET pin is at V_{SS}, deep power-down mode is enabled which minimizes power consumption and provides write protection during reset. A reset time (tPHQV) is required from #RESET switching high until outputs are valid. Likewise, the device has a wake time (tPHEL) from #RESET-high until writes to the CUI are recognized. With #RESET at V_{SS}, the WSM is reset and the status register is cleared.

The device is available in 48-lead TSOP (Thin Small Outline Package, 1.2 mm thick). Pinout is shown in Figure 2.

4. BLOCK DIAGRAM

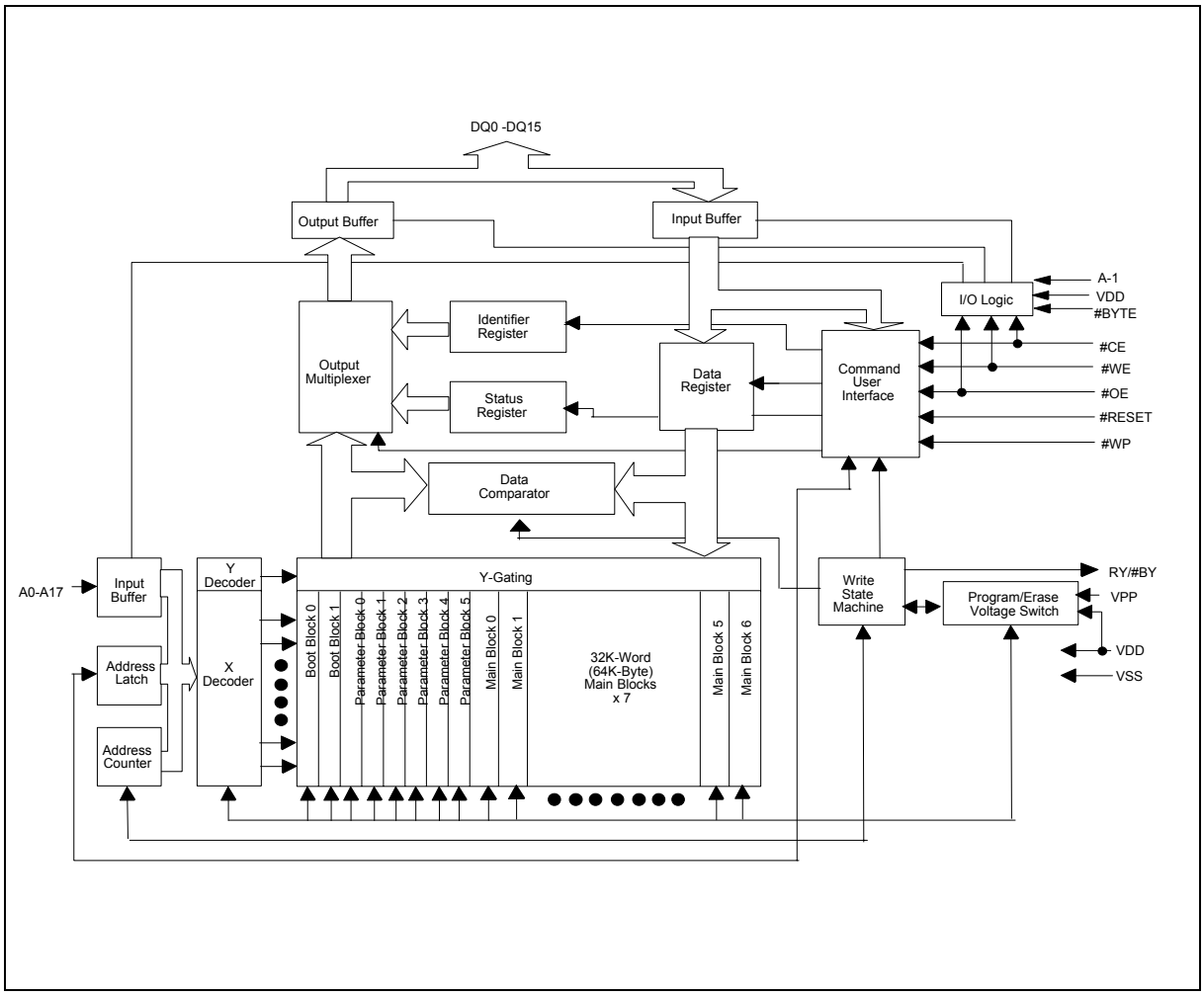


Figure 1. Block Diagram

5. PIN CONFIGURATION

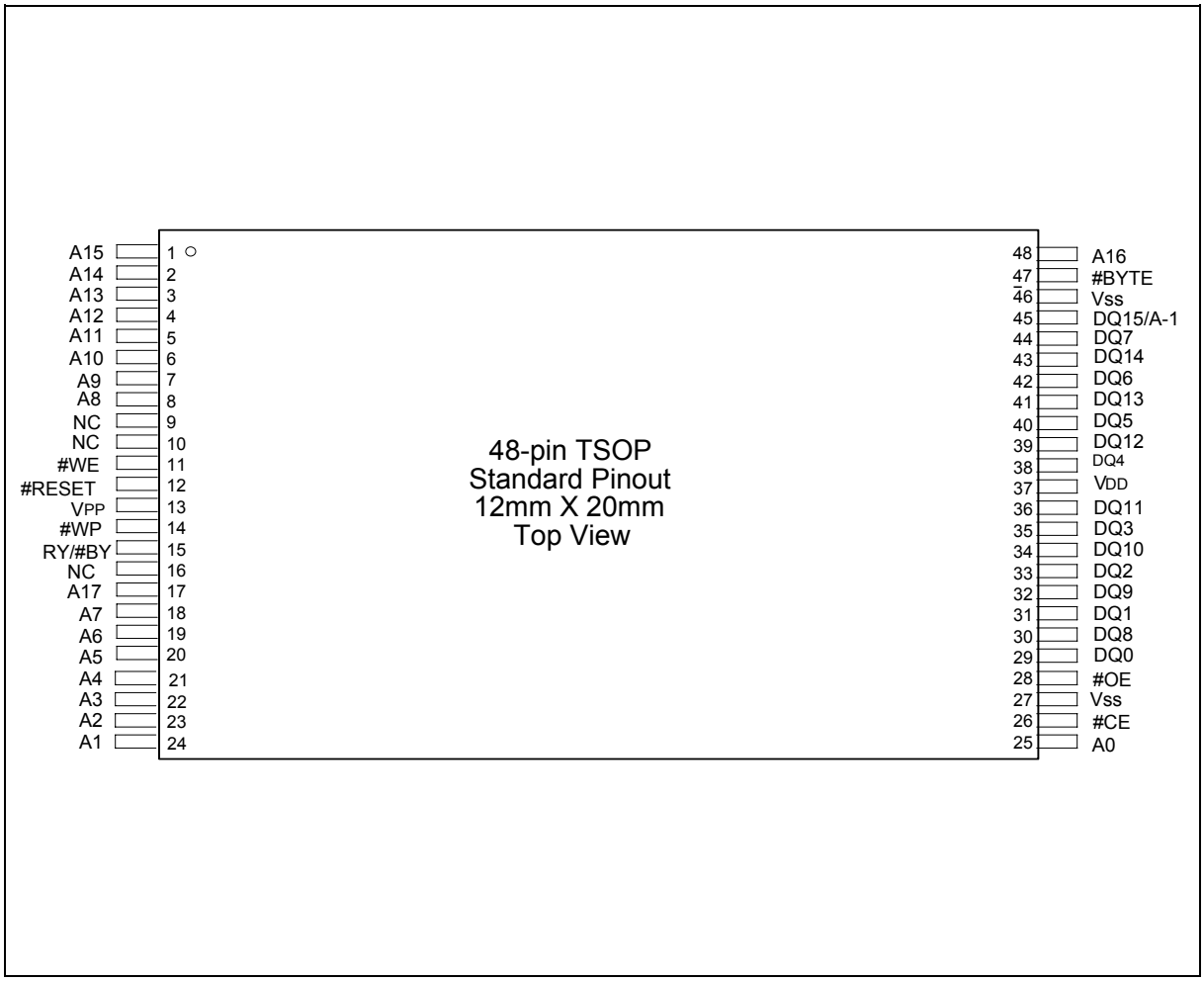


Figure 2. TSOP 48-Lead Pinout

6. PIN DESCRIPTION

SYM.	TYPE	NAME AND FUNCTION
A – 1 A0 – A17	INPUT	**ADDRESS INPUTS**: Addresses are internally latched during a write cycle. A – 1: Byte Select Address. Not used in × 16 mode. A0 – A10: Row Address. Selects 1 of 2048 word lines. A11 – A14: Column Address. Selects 1 of 16 bit lines. A15 – A17: Main Block Address. (Boot and Parameter block Addresses are A12 – A17.)
DQ0 – DQ15	INPUT/ OUTPUT	**DATA INPUT/OUTPUTS**: DQ0 – DQ7:Inputs data and commands during CUI write cycles; outputs data during memory array, status register and identifier code read cycles. Data pins float to high-impedance when the chip is deselected or outputs are disabled. Data is internally latched during a write cycle. DQ8 – DQ15:Inputs data during CUI write cycles in × 16 mode; outputs data during memory array read cycles in × 16 mode; not used for status register and identifier code read mode. Data pins float to high-impedance when the chip is deselected, outputs are disabled, or in × 8 mode (#Byte = V_{IL}). Data is internally latched during a write cycle.
#CE	INPUT	**CHIP ENABLE**: Activates the device's control logic, input buffers, decoders and sense amplifiers. #CE-high deselects the device and reduces power consumption to standby levels.
#RESET	INPUT	**RESET/DEEP POWER-DOWN**: Puts the device in deep power-down mode and resets internal automation. #RESET-high enables normal operation. When driven low, #RESET inhibits write operations which provides data protection during power transitions. Exit from deep power-down sets the device to read array mode. With #RESET = V_{HH}, block erase or word/byte write can operate to all blocks without #WP state. Block erase or word/byte write with V_{IH} < #RESET < V_{HH} produce spurious results and should not be attempted.
#OE	INPUT	**OUTPUT ENABLE**: Gates the device's outputs during a read cycle.
#WE	INPUT	**WRITE ENABLE**: Controls writes to the CUI and array blocks. Addresses and data are latched on the rising edge of the #WE pulse.
#WP	INPUT	**WRITE PROTECT**: Master control for boot blocks locking. When $V_{IL,}$ locked boot blocks cannot be erased and programmed.
#BYTE	INPUT	**BYTE ENABLE**: #BYTE V_{IL} places the device in byte mode (× 8), All data is then input or output on DQ0 – 7, and DQ8 – 15 float. #BYTE V_{IH} places the device in word mode (× 16), and turns off the A-1 input buffer.
RY/#BY	OUTPUT	**READY/#BUSY**: Indicates the status of the internal WSM. When low, the WSM is performing an internal operation (block erase or word/byte write). RY/#BY-high indicates that the WSM is ready for new commands, block erase is suspended, and word/byte write is inactive, word/byte write is suspended, or the device is in deep power-down mode. RY/#BY is always active and does not float when the chip is deselected or data outputs are disabled.
VPP	SUPPLY	**BLOCK ERASE AND WORD/BYTE WRITE POWER SUPPLY**: For erasing array blocks or writing words/bytes. With $V_{PP} \le V_{PPLK}$, memory contents cannot be altered. Block erase and word/byte write with an invalid V_{PP} (see DC Characteristics) produce spurious results and should not be attempted.
V_{DD}	SUPPLY	**DEVICE POWER SUPPLY**: Internal detection configures the device for 2.7V, 3.3V or 5V operation. To switch from one voltage to another, ramp V_{DD} down to V_{SS} and then ramp V_{DD} to the new voltage. Do not float any power pins. With $V_{DD} \le$ VLKO, all write attempts to the flash memory are inhibited. Device operations at invalid V_{DD} voltage (see DC Characteristics) produce spurious results and should not be attempted.
V_{SS}	SUPPLY	**GROUND**: Do not float any ground pins.
NC		**NO CONNECT**: Lead is not internal connected; it may be driven or floated.

Table 1.

7. PRINCIPLES OF OPERATION

The W28V400B/T SmartVoltage Flash memory includes an on-chip WSM to manage block erase and word/byte write functions. It allows for 100 percent TTL-level control inputs, fixed power supplies during block erase, full chip erase, word/byte write and lock-bit configuration, and minimal processor overhead with RAM-like interface timings.

After initial device power-up or return from reset mode (see Bus Operations section), the device defaults to read array mode. Manipulation of external memory control pins allow array read, standby and output disable operations.

Status register and identifier codes can be accessed through the CUI independent of the V_{PP} voltage. High voltage on V_{PP} enables successful block erase, word/byte writing. All functions associated with altering memory contents (block erase, word/byte write, status and identifier codes) are accessed via the CUI and verified through the status register.

Commands are written using standard microprocessor write timings. The CUI contents serve as input to the WSM, which controls the block erase and word/byte write. The internal algorithms are regulated by the WSM, including pulse repetition, internal verification and margining of data. Addresses and data are internally latched during write cycles. Writing the appropriate command outputs array data, accesses the identifier codes, or outputs status register data.

Interface software that initiates and polls progress of block erase and word/byte write can be stored in any block. This code is copied to and executed from system RAM during flash memory updates. After successful completion, reads are again possible via the Read Array command. Block erase suspend allows system software to suspend a block erase to read/write data from/to blocks other than that which is suspend. Word/byte write suspend allows system software to suspend a word/byte write to read data from any other flash memory array location.

Data Protection

Depending on the application, the system designer may choose to make the V_{PP} power supply switchable (available only when memory block erases or word/byte writes are required) or hardwired to $V_{PPH1/2/3}$. The device accommodates either design practice and encourages optimization of the processor-memory interface.

When $V_{PP} \leq V_{PPLK}$, memory contents cannot be altered. The CUI, with two-step block erase or word/byte write command sequences, provides protection from unwanted operations even when high voltage is applied to V_{PP}. All write functions are disabled when V_{DD} is below the write lockout voltage V_{LKO} or when #RESET is at V_{IL}. The device's boot blocks locking capability for #WP provides additional protection from inadvertent code or data alteration by block erase and word/byte write operations.

Refer to Table 6 for write protection alternatives.

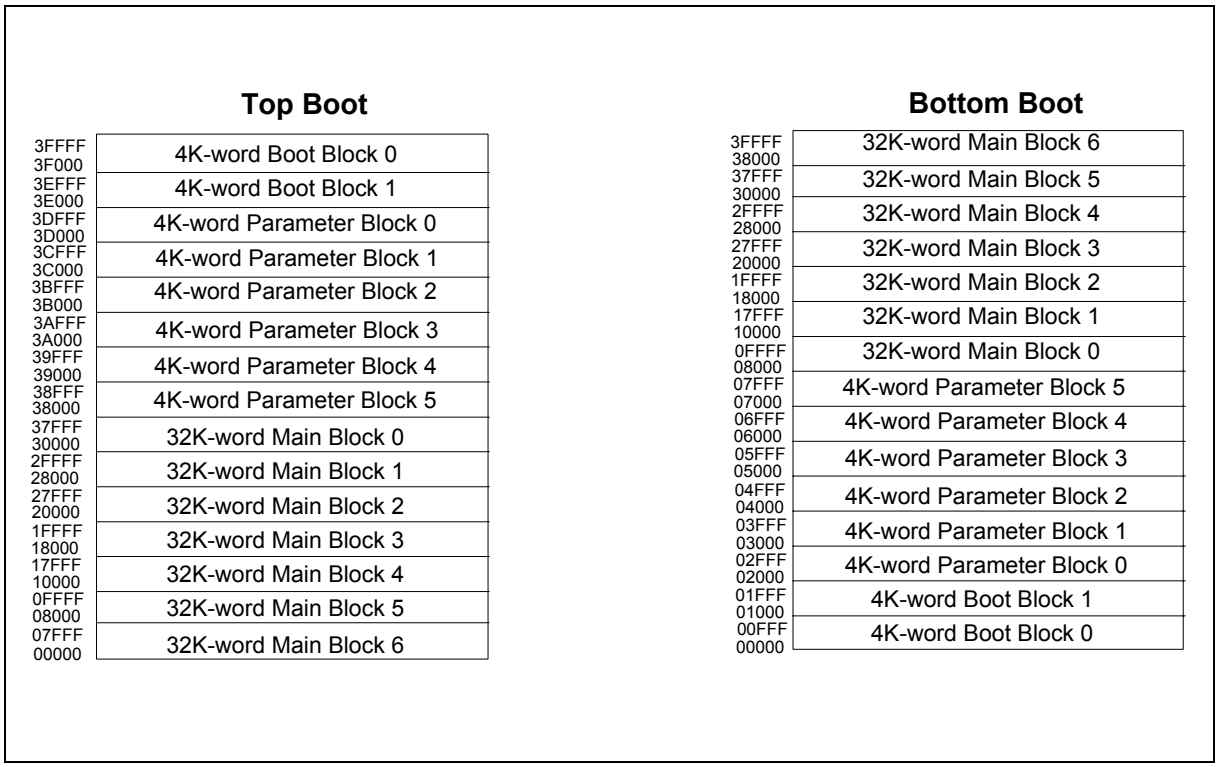


Figure 3. Memory Map

8. BUS OPERATION

The local CPU reads and writes flash memory in-system. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles.

Read

Information can be read from any block, identifier codes or status register independent of the V_{PP} voltage. #RESET can be at either V_{IH} or V_{HH}.

The first task is to write the appropriate read mode command (Read Array, Read Identifier Codes or Read Status Register) to the CUI. Upon initial device power-up or after exit from deep power-down mode, the device automatically resets to read array mode. Six control pins dictate the data flow in and out of the component: #CE, #OE, #WE, #RESET, #WP and #BYTE. #CE and #OE must be driven active to obtain data at the outputs. #CE is the device selection control, and when active enables the selected memory device. #OE is the data output (DQ0 – DQ15) control and when active drives the selected memory data onto the I/O bus. #WE must be at V_{IH} and #RESET must be at V_{IH} or V_{HH}. Figure 13, 14 illustrates read cycle.

Output Disable

With #OE at a logic-high level (V_{IH}), the device outputs are disabled. Output pins (DQ0 – DQ15) are placed in a high-impedance state.

Standby

Setting #CE to a logic-high level (V_{IH}) deselects the device and places it in standby mode, which substantially reduces device power consumption. DQ0 – DQ15 outputs are placed in a high impedance state independent of #OE. If deselected during block erase or word/byte write, the device continues functioning, and it continues to consume active power until the operation is completed.

Deep Power-down

Setting #RESET to V_{IL} initiates the deep power-down mode.

In read modes, setting #RESET at V_{IL} deselects the memory, places output drivers in a high-impedance state and turns off all internal circuits. #RESET must be held low for a minimum of 100 nS. A delay (t_{PHQV}) is required after return from reset until initial memory access outputs are valid. After this wake-up interval, normal operation is restored. The CUI is reset to read array mode status register is set to 80H.

During block erase or word/byte write modes, #RESET at V_{IL} will abort the operation. RY/#BY remains low until the reset operation is complete. Memory contents at the aborted location are no longer valid since the data may be partially erased or written. A delay (t_{PHWL}) is required after #RESET goes to logic-high (V_{IH}) before another command can be written.

As with any automated device, it is important to assert #RESET during system reset. When the system comes out of reset, it expects to read from the flash memory. Automated flash memories provide status information when accessed during block erase or word/byte write modes. If a CPU reset occurs with no flash memory reset, proper CPU initialization may not occur because the flash memory may be providing status information instead of array data.

Winbond's flash memories allow proper CPU initialization following a system reset through the use of the #RESET input. In this application, #RESET is controlled by the same #RESET signal that resets the system CPU.

Read Identifier Codes Operation

The read identifier codes operation outputs the manufacturer code and device code (refer to Figure 4). Using the manufacturer and device codes, the system CPU can automatically match the device with its proper algorithms.

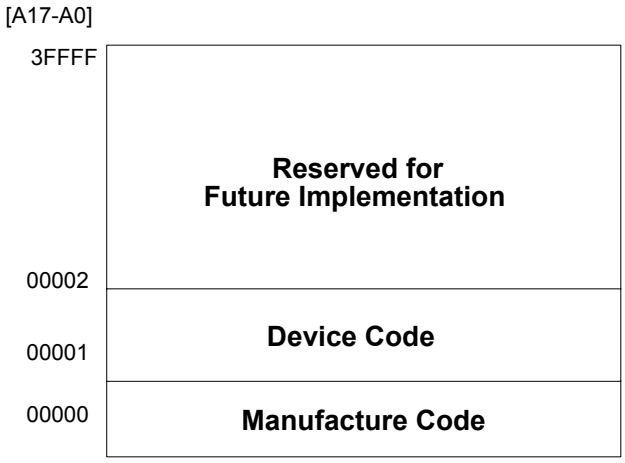


Figure 4. Device Identifier Code Memory Map

Write

Writing commands to the CUI enable reading of device data and identifier codes. They also control inspection and clearing of the status register. When $V_{DD} = V_{DD1/2/3/4}$ and used. $V_{PP} = V_{PPH1/2/3}$, the CUI additionally controls block erasure and word/byte write.

The Block Erase command requires appropriate command data and an address within the block to be erased. The Word/Byte Write command requires the command and address of the location to be written.

The CUI does not occupy an addressable memory location. A write occurs when #WE and #CE are active (low). The address and data needed to execute a command are latched on the rising edge of #WE or #CE, whichever occurs first. Standard microprocessor write timings are used.

Figures 15 and 16 illustrate #WE and #CE controlled write operations.

9. COMMAND DEFINITIONS

When $V_{PP} \leq V_{PPLK}$, read operations from the status register, identifier codes, or blocks are enabled. Setting $V_{PPH1/2/3} = V_{PP}$ enables successful block erase and word/byte write operations.

Device operations are selected by writing specific commands into the CUI. Table 4 defines these commands.

Table 3.1. Bus Operations (#BYTE = V_{IH}) (Note 1, 2)

MODE	#RESET	#CE	#OE	#WE	ADDRESS	V_{PP}	DQ0 – 15	RY/#BY(3)
Read (Note 8)	V_{IH} or V_{HH}	V_{IL}	V_{IL}	V_{IH}	X	X	DOUT	X
Output Disable	V_{IH} or V_{HH}	V_{IL}	V_{IH}	V_{IH}	X	X	High Z	X
Standby (Note 10)	V_{IH} or V_{HH}	V_{IH}	X	X	X	X	High Z	X
Deep Power-down (Note 4, 10)	V_{IL}	X	X	X	X	X	High Z	VOH
Read Identifier Codes (Note 8)	V_{IH} or V_{HH}	V_{IL}	V_{IL}	V_{IH}	See Figure 4	X	Note 5	VOH
Write (Note 6, 7, 8)	V_{IH} or V_{HH}	V_{IL}	V_{IH}	V_{IL}	X	X	DIN	X

Table 3.2. Bus Operations (#BYTE = V_{IL}) (Note 1, 2)

MODE	#RESET	#CE	#OE	#WE	ADDRESS	V_{PP}	DQ0 – 7	DQ8 – 15	RY/#BY(3)
Read (Note 8)	V_{IH} or V_{HH}	V_{IL}	V_{IL}	V_{IH}	X	X	DOUT	High Z	X
Output Disable	V_{IH} or V_{HH}	V_{IL}	V_{IH}	V_{IH}	X	X	High Z	High Z	X
Standby (Note 10)	V_{IH} or V_{HH}	V_{IH}	X	X	X	X	High Z	High Z	X
Deep Power-down (Note 4, 10)	V_{IL}	X	X	X	X	X	High Z	High Z	VOH
Read Identifier Codes (Note 8, 9)	V_{IH} or V_{HH}	V_{IL}	V_{IL}	V_{IH}	See Figure 4	X	Note 5	High Z	VOH
Write (Note 6, 7, 8)	V_{IH} or V_{HH}	V_{IL}	V_{IH}	V_{IL}	X	X	DIN	X	X

Notes:

1. Refer to DC Characteristics. When $V_{PP} \leq V_{PPLK}$, memory contents can be read, but not altered.
2. X can be V_{IL} or V_{IH} for control pins and addresses, and V_{PPLK} or $V_{PPH1/2/3}$ for V_{PP}. See DC Characteristics for V_{PPLK} and $V_{PPH1/2/3}$ voltages.
3. RY/#BY is V_{OL} when the WSM is executing internal block erase or word/byte write algorithms. It is V_{OH} during when the WSM is not busy, in block erase suspend mode (with word/byte write inactive), word/byte write suspend mode or deep power-down mode.
4. #RESET at $V_{SS} \pm 0.2V$ ensures the lowest deep power-down current.
5. See Read Identifier Codes Command section for details.
6. Command writes involving block erase or word/byte write are reliably executed when $V_{PP} = V_{PPH1/2/3}$ and $V_{DD} = V_{DD1/2/3/4}$. Block erase or word/byte write with $V_{IH} <$ #RESET $< V_{HH}$ produce spurious results and should not be attempted.
7. Refer to Table 4 for valid DIN during a write operation.
8. Never hold #OE low and #WE low at the same timing.
9. A-1 set to V_{IL} or V_{IH} in byte mode (#BYTE = V_{IL}).
10. #WP set to V_{IL} or V_{IH}.

Table 4. Command Definitions(10)

COMMAND	BUS CYCLES REQ'D.	FIRST BUS CYCLE			SECOND BUS CYCLE		
		Oper(1)	Addr(2)	Data(3)	Oper(1)	Addr(2)	Data(3)
Read Array/Reset	1	Write	X	FFH			
Read Identifier Codes	≥2 (Note 4)	Write	X	90H	Read	IA	ID
Read Status Register	2	Write	X	70H	Read	X	SRD
Clear Status Register	1	Write	X	50H			
Block Erase	2 (Note 5)	Write	BA	20H	Write	BA	D0H
Word/Byte Write	2 (Note 5, 6)	Write	WA	40H or 10H	Write	WA	WD
Block Erase and Word/Byte Write Suspend	1 (Note 5)	Write	X	B0H			
Block Erase and Word/Byte Write Resume	1 (Note 5)	Write	X	D0H			

Notes:

1. BUS operations are defined in Table 3.1 and Table 3.2.
2. X = Any valid address within the device.
   IA = Identifier Code Address: see Figure 4. A-1 set to V_{IL} or V_{IH} in Byte Mode (#BYTE = V_{IL}).
   BA = Address within the block being erased. The each block can select by the address pin A17 through A12 combination.
   WA = Address of memory location to be written.
3. SRD = Data read from status register. See Table 7 for a description of the status register bits.
   WD = Data to be written at location WA. Data is latched on the rising edge of #WE or #CE (whichever goes high first).
   ID = Data read from identifier codes.
4. Following the Read Identifier Codes command, read operations access manufacturer and device codes. See Read Identifier Codes Command section for details.
5. If the block is boot block, #WP must be at V_{IH} or #RESET must be at V_{HH} to enable block erase or word/byte write operations. Attempts to issue a block erase or word/byte write to a boot block while #WP is V_{IH} or #RESET is V_{IH}.
6. Either 40H or 10H are recognized by the WSM as the word/byte write setup.
7. Commands other than those shown above are reserved by Winbond for future device implementations and should not be used.

Read Array Command

Upon initial device power-up and after exit from deep power-down mode, the device defaults to read array mode. This operation is also initiated by writing the Read Array command. The device remains enabled for reads until another command is written. Once the internal WSM has started a block erase or word/byte write, the device will not recognize the Read Array command until the WSM completes its operation unless the WSM is suspended via an Erase Suspend or Word/Byte Write Suspend command.

The Read Array command functions independently of the V_{PP} voltage and #RESET can be V_{IH} or V_{HH}.

Read Identifier Codes Command

The identifier code operation is initiated by writing the Read Identifier Codes command. Following the command write, read cycles from addresses shown in Figure 4 retrieve the manufacturer and device codes (see Table 5 for identifier code values). To terminate the operation, write another valid command. Like the Read Array command, the Read Identifier Codes command functions independently of the V_{PP} voltage and #RESET can be V_{IH} or V_{HH}. Following the Read Identifier Codes command, the following information can be read:

Table 4. Identifier Codes

CODE		ADDRESS [A17 – A0]	DATA [DQ7 – DQ0]
Manufacture Code		00000H	B0H
Device Code	Top Boot	00001H	58H
	Bottom Boot		5AH

Read Status Register Command

The status register may be read to determine when a block erase or word/byte write is complete and whether the operation completed successfully. It may be read at any time by writing the Read Status Register command. After writing this command, all subsequent read operations output data from the status register until another valid command is written. The status register contents are latched on the falling edge of #OE or #CE, whichever occurs. #OE or #CE must toggle to V_{IH} before further reads to update the status register latch. The Read Status Register command functions independently of the V_{PP} voltage. #RESET can be V_{IH} or V_{HH}.

Clear Status Register Command

Status register bits SR.5, SR.4, SR.3 or SR.1 are set to "1"s by the WSM and can only be reset by the Clear Status Register command. These bits indicate various failure conditions (see Table 7). By allowing system software to reset these bits, several operations (such as cumulatively erasing multiple blocks or writing several words/bytes in sequence) may be performed. The status register may be polled to determine if an error occurred during the sequence. To clear the status register, the Clear Status Register command (50H) is written. It functions independently of the applied V_{PP} voltage. #RESET can be V_{IH} or V_{HH}. This command is not functional during block erase or word/byte write suspend modes.

Block Erase Command

Erase is executed one block at a time and initiated by a two-cycle command. A block erase setup is first written, followed by an block erase confirm. This command sequence requires appropriate sequencing and an address within the block to be erased (erase changes all block data to FFFFH). Block preconditioning, erase, and verify are handled internally by the WSM (invisible to the system).

After the two-cycle block erase sequence is written, the device automatically outputs status register data when read (see Figure 5). The CPU can detect block erase completion by analyzing the output data of the RY/#BY pin or status register bit SR.7.

When the block erase is complete, status register bit SR.5 should be checked. If a block erase error is detected, the status register should be cleared before system software attempts corrective actions. The CUI remains in read status register mode until a new command is issued.

This two-step command sequence of set-up followed by execution ensures that block contents are not accidentally erased. An invalid Block Erase command sequence will result in both status register bits SR.4 and SR.5 being set to "1". Also, reliable block erasure can only occur when $V_{DD} = V_{DD1/2/3/4}$ and $V_{PP} = V_{PPH1/2/3}$. In the absence of this high voltage, block contents are protected against erasure.

If block erase is attempted while $V_{PP} \leq V_{PPLK}$, SR.3 and SR.5 will be set to "1". Successful block erase for boot blocks requires that the corresponding if set, that #WP = V_{IH} or #RESET = V_{HH}. If block erase is attempted to boot block when the corresponding #WP = V_{IL} or #RESET = V_{IH}, SR.1 and SR.5 will be set to "1". Block erase operations with V_{IH} < #RESET < V_{HH} produce spurious results and should not be attempted.

Word/Byte Write Command

Word/byte write is executed by a two-cycle command sequence. Word/byte write setup (standard 40H or alternate 10H) is written, followed by a second write that specifies the address and data (latched on the rising edge of #WE). The WSM then takes over, controlling the word/byte write and write verify algorithms internally. After the word/byte write sequence is written, the device automatically outputs status register data when can be read (see Figure 6). The CPU can detect the completion of the word/byte write event by analyzing the RY/#BY pin or status register bit SR.7.

When word/byte write is complete, status register bit SR.4 should be checked. If word/byte write error is detected, the status register should be cleared. The internal WSM verify only detects errors for "1"s that do not successfully write to "0"s. The CUI remains in read status register mode until it receives another command.

Reliable word/byte writes can only occur when $V_{DD} = V_{DD1/2/3/4}$ and $V_{PP} = V_{PPH1/2/3}$. In the absence of this high voltage, memory contents are protected against word/byte writes. If word/byte write is attempted while $V_{PP} \leq V_{PPLK}$, status register bits SR.3 and SR.4 will be set to "1". Successful word/byte write for boot blocks requires that the corresponding if set, that #WP = V_{IH} or #RESET = V_{HH}. If word/byte write is attempted to boot block when the corresponding #WP= V_{IL} or #RESET= V_{IH}, SR.1 and SR.4 will be set to "1". Word/byte write operations with V_{IH} < #RESET < V_{HH} produce spurious results and should not be attempted.

Block Erase Suspend Command

The Block Erase Suspend command allows block-erase interruption to read or word/byte write data in another block of memory. Once the block-erase process starts, writing the Block Erase Suspend command requests that the WSM suspend the block erase sequence at a predetermined point in the algorithm. The device outputs status register data when read after the Block Erase Suspend command is written. Polling status register bits SR.7 and SR.6 can determine when the block erase operation has been suspended (both will be set to "1"). RY/#BY will also transition to V_{OH}. Specification t_{WHRH2} defines the block erase suspend latency.

At this point, a Read Array command can be written to read data from blocks other than that which is suspended. A Word/Byte Write command sequence can also be issued during erase suspend to program data in other blocks. Using the Word/Byte Write Suspend command (see Word/Byte Write Suspend Command section), a word/byte write operation can also be suspended. During a word/byte write operation with block erase suspended, status register bit SR.7 will return to "0" and the RY/#BY output will transition to V_{OL}. However, SR.6 will remain "1" to indicate block erase suspend status.

The only other valid commands while block erase is suspended are Read Status Register and Block Erase Resume. After a Block Erase Resume command is written to the flash memory, the WSM will continue the block erase process. Status register bits SR.6 and SR.7 will automatically clear and RY/#BY will return to V_{OL}. After the Erase Resume command is written, the device automatically outputs status register data when read (see Figure 7). V_{PP} must remain at $V_{PPH1/2/3}$ (the same V_{PP} level used for block erase) while block erase is suspended. #RESET must also remain at V_{IH} or V_{HH} (the same #RESET level used for block erase). #WP must also remain at V_{IL} or V_{IH} (the same #WP level used for block erase). Block erase cannot resume until word/byte write operations initiated during block erase suspend have completed.

Word/Byte Write Suspend Command

The Word/Byte Write Suspend command allows word/byte write interruption to read data in other flash memory locations. Once the word/byte write process starts, sending the Word/Byte Write Suspend command causes the WSM to suspend the word/byte write sequence at a predetermined point in the algorithm. The device continues to output status register data when read after the Word/Byte Write Suspend command is written. Polling status register bits SR.7 and SR.2 can determine when the word/byte write operation has been suspended (both will be set to "1"). RY/#BY will also transition to V_{OH}. Specification t_{WHRH1} defines the word/byte write suspend latency.

At this point, a Read Array command can be written to read data from locations other than that which is suspended. The only other valid commands while word/byte write is suspended are Read Status Register and Word/Byte Write Resume. After Word/Byte Write Resume command is written to the flash memory, the WSM will continue the word/byte write process. Status register bits SR.2 and SR.7 will automatically clear and RY/#BY will return to V_{OL}. After the Word/Byte Write Resume command is written, the device automatically outputs status register data when read (see Figure 8). V_{PP} must remain at $V_{PPH1/2/3}$ (the same V_{PP} level used for word/byte write) while in word/byte write suspend mode. #RESET must also remain at V_{IH} or V_{HH} (the same #RESET level used for word/byte write). #WP must also remain at V_{IL} or V_{IH} (the same #WP level used for word/byte write).

Considerations of Suspend

After the suspend command write to the CUI, read status register command has to write to CUI, then status register bit SR.6 or SR.2 should be checked for places the device in suspend mode.

Block Locking

This Boot Block Flash memory architecture features two hardware-lockable boot blocks so that the kernel code for the system can be kept secure while other blocks are programmed or erased as necessary.

$V_{PP} = V_{IL}$ for Complete Protection

The V_{PP} programming voltage can be held low for complete write protection of all blocks in the flash device.

#WP = V_{IL} for Block Locking

The lockable blocks are locked when #WP = V_{IL}; any program or erase operation to a locked block will result in an error, which will be reflected in the status register. For top configuration, the top two boot blocks are lockable. For the bottom configuration, the bottom two boot blocks are lockable. Unlocked blocks can be programmed or erased normally (Unless V_{PP} is below V_{PPLK}).

#WP = V_{IH} for Block Unlocking

#WP = V_{IH} unlocks all lockable blocks.

These blocks can now be programmed or erased.

#WP controls 2 boot blocks locking and V_{PP} provides protection against spurious writes. Table 6 defines the write protection methods.

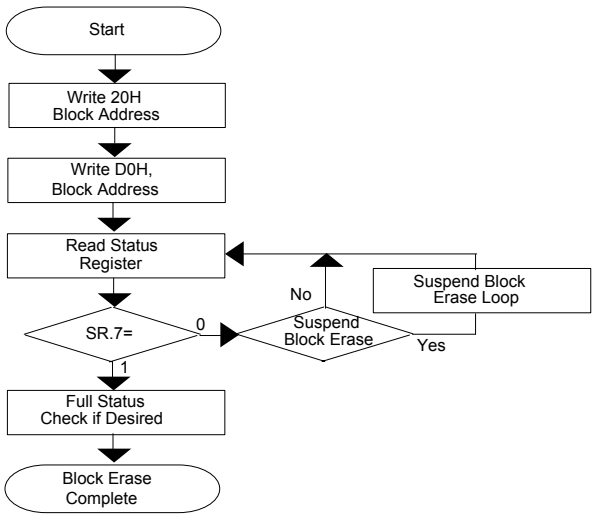
Table 6. Write Protection Alternatives

OPERATION	V_{PP}	#RESET	#WP	EFFECT
Block Erase or Word/Byte Write	V_{IL}	X	X	All Blocks Locked.
	> V_{PPLK}	V_{IL}	X	All Blocks Locked.
		V_{HH}	X	All Blocks Unlocked.
		V_{HH}	V_{IL}	2 Boot Blocks Locked.
			V_{IH}	All Blocks Unlocked.

Table 7. Status Register Definition

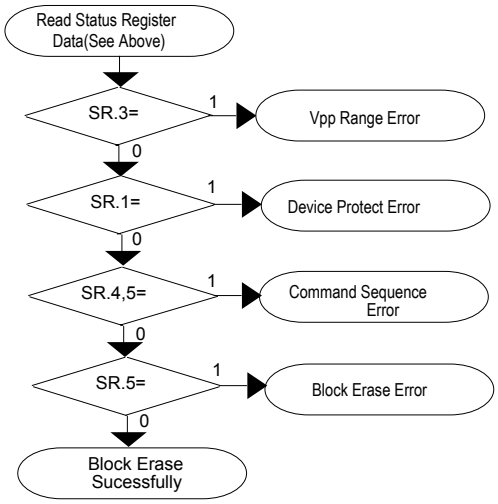
WSMS	ESS	ES	WBWS	VPPS	WBWSS	DPS	R
7	6	5	4	3	2	1	0

	Notes:
SR.7 = WRITE STATE MACHINE STATUS (WSMS) 1 = Ready 0 = Busy	Check RY/#BY or SR.7 to determine block erase or word/byte write completion. SR.6-0 are invalid while SR.7 = "0".
SR.6 = ERASE SUSPEND STATUS (ESS) 1 = Block Erase Suspended 0 = Block Erase in Progress/Completed	
SR.5 = ERASE STATUS (ES) 1 = Error in Block Erase 0 = Successful Block Erase	If both SR.5 and SR.4 are "1"s after a block erase attempt, an improper command sequence was entered.
SR.4 = WORD/BYTE WRITE STATUS (WBWSLBS) 1 = Error in Word/Byte Write 0 = Successful Word/Byte Write	
SR.3 = V_{PP} STATUS (VPPS) 1 = V_{PP} Low Detect, Operation Abort 0 = V_{PP} OK	SR.3 does not provide a continuous indication of V_{PP} level. The WSM interrogates and indicates the V_{PP} level only after Block Erase or Word/Byte Write command sequences. SR.3 is not guaranteed to reports accurate feedback only when $V_{PP} \neq V_{PPH1/2/3}$.
SR.2 = WORD/BYTE WRITE SUSPEND STATUS (WBWSS) 1 = Word/Byte Write Suspended 0 = Word/Byte Write in Progress/Completed	The WSM interrogates the #WP and #RESET only after Block Erase or Word/Byte Write command sequences. It informs the system, depending on the attempted operation, if the #WP is not V_{IH}, #RESET is not V_{HH}.
SR.1 = DEVICE PROTECT STATUS (DPS) 1 = WP# or RP# Lock Detected, Operation Abort 0 = Unlock	
SR.0 = RESERVED FOR FUTURE ENHANCEMENTS (R)	SR.0 is reserved for future use and should be masked out when polling the status register.



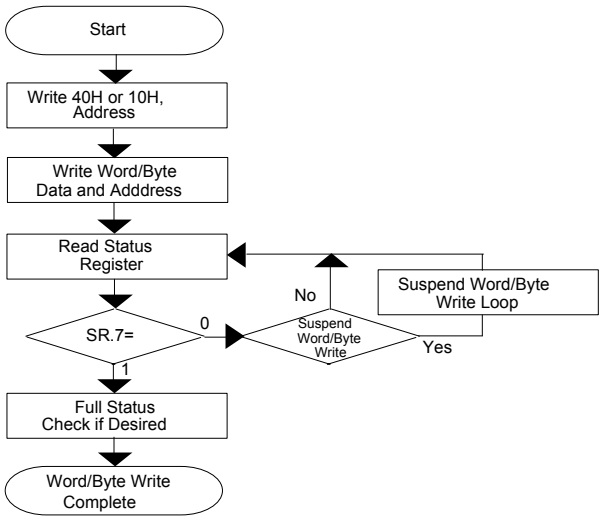
Bus Operation	Command	Comments
Write	Erase Setup	Data = 20H Addr = Within Block to be Erased
Write	Erase Confirm	Data = D0H Addr = Within Block to be Erased
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Repeat for subsequent block erasures. Full status check can be done after each block erase or after a sequence of block erasures. Write FFH after the last operation to place device in read array mode.		

Full STATUS CHECK PROCEDURE



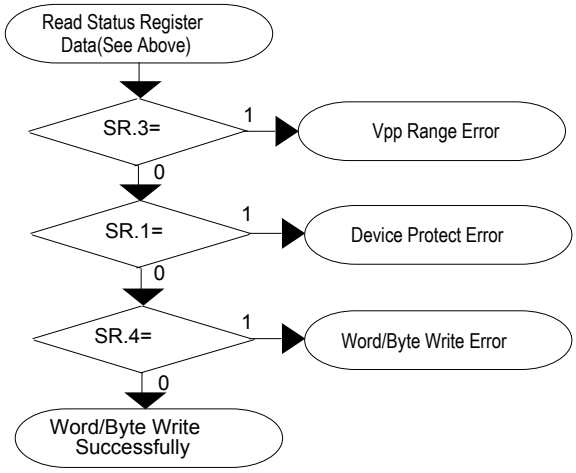
Bus Operation	Command	Comments
Standby		Check SR.3 1 = V_{PP} Error Detect
Standby		Check SR.1 1 = Device Protect Detect
Standby		Check SR.4, 5 Both 1 = Command Sequence Error
Standby		Check SR.5 1 = Block Erase Error
SR.5, SR.4, SR.3 and SR.1 are only cleared by the Clear Status. Register Command in cases where multiple blocks are erased before full status is checked. If error is detected, clear the Status Register before attempting retry or other error recovery.		

Figure 5. Automated Block Erase Flowchart



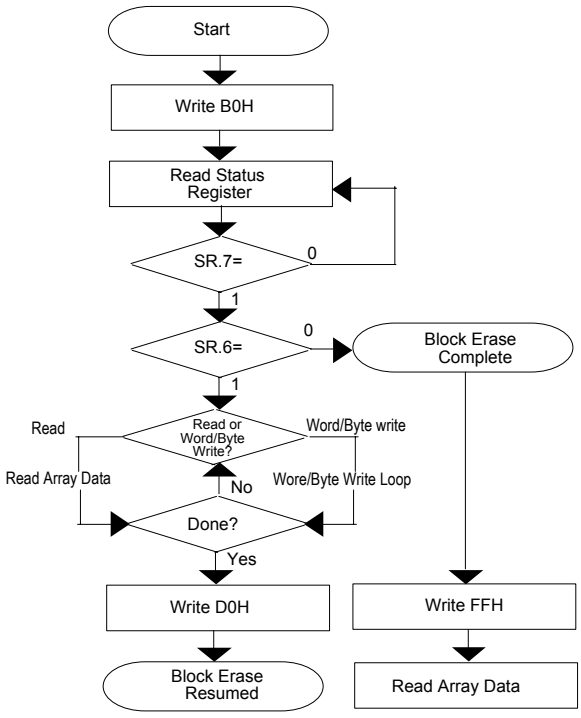
Bus Operation	Command	Comments
Write	Setup Word/Byte Write	Data = 40H or 10H Addr = Location to Be Written
Write	Word/Byte Write	Data = Data to Be Written Addr = Location to Be Written
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Repeat for subsequent byte writes. SR full status check can be done after each Word/Byte write, or after a sequence of Word/Byte writes. Write FFH after the last Word/Byte write operation to place device in read array mode.		

Full STATUS CHECK PROCEDURE



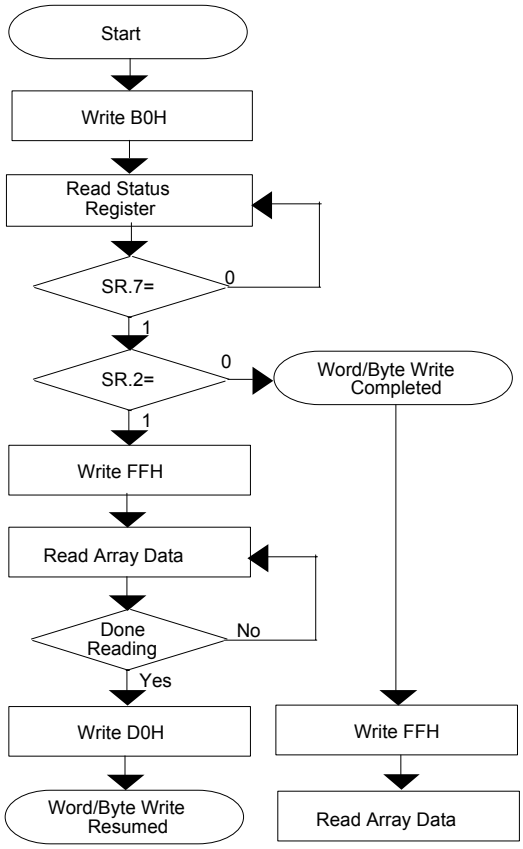
Bus Operation	Command	Comments
Standby		Check SR.3 1 = V_{PP} Error Detect
Standby		Check SR.1 1 = Device Protect Detect
Standby		Check SR.4 1 = Data Write Error
SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register command in cases where multiple locations are written before full status is checked. If error is detected, clear the Status Register before attempting retry or other error recovery.		

Figure 6. Automated Word/Byte Write Flowchart



Bus Operation	Command	Comments
Write	Erase Suspend	Data = B0H Addr = X
Read		Status Register Data Addr = X
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Standby		Check SR.6 1 = Block Erase Suspended 0 = Block Erase Completed
Write	Erase Resume	Data = D0H Addr = X

Figure 7. Block Erase Suspend/Resume Flowchart



Bus Operation	Command	Comments
Write	Word/Byte Write Suspend	Data = B0H Addr = X
Read		Status Register Data Addr = X
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Standby		Check SR.2 1 = Word/Byte Write Suspended 0 = Word/Byte Write Completed
Write	Read Array	Data = FFH Addr = X
Read		Read Array locations other than that being written.
Write	Word/Byte Write Resume	Data = D0H Addr = X

Figure 8. Word/Byte Write Suspend/Resume Flowchart

10. DESIGN CONSIDERATIONS

Three-line Output Control

This device will often be used in large memory arrays. Winbond provides three control inputs to accommodate multiple memory connections. Three-line control provides for:

a. Lowest possible memory power dissipation.

b. Complete assurance that data bus contention will not occur.

To use these control inputs efficiently, an address decoder should enable #CE while #OE should be connected to all memory devices and the system's #READ control line. This assures that only selected memory devices have active outputs while deselected memory devices are in standby mode. #RESET should be connected to the system POWERGOOD signal to prevent unintended writes during system power transitions. POWERGOOD should also toggle during system reset.

RY/#BY, Block Erase and Word/Byte Write Polling

RY/#BY is a full CMOS output that provides a hardware method of detecting block erase and word/byte write completion. It transitions low after block erase or word/byte write commands and returns to V_{OH} when the WSM has finished executing the internal algorithm.

RY/#BY can be connected to an interrupt input of the system CPU or controller. It is active at all times. RY/#BY is also V_{OH} when the device is in block erase suspend (with word/byte write inactive), word/byte write suspend or deep power-down modes.

Power Supply Decoupling

Flash memory power switching characteristics require careful device decoupling. System designers are interested in three supply current issues; standby current levels, active current levels and transient peaks produced by falling and rising edges of #CE and #OE. Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks.

Each device should have a 0.1 μF ceramic capacitor connected between V_{DD} and V_{SS} and between V_{PP} and V_{SS}. These high frequency, low inductance capacitors should be placed as close as possible to package leads. Additionally, for every eight devices, a 4.7 μF electrolytic capacitor should be placed at the array's power supply connection between V_{DD} and V_{SS}. The bulk capacitor will overcome voltage drops caused by PC board trace inductance.

V_{PP} Trace on Printed Circuit Boards

Updating flash memories that reside in the target system requires that the printed circuit board designer pay attention to the V_{PP} power supply trace. The V_{PP} pin supplies the memory cell current for word/byte writing and block erasing. Use similar trace widths and layout considerations given to the V_{DD} power bus. Adequate V_{PP} supply traces and decoupling will decrease V_{PP} voltage spikes and overshoots.

V_{DD}, V_{PP}, #RESET Transitions

Block erase and word/byte write are not guaranteed if V_{PP} falls outside of a valid $V_{PPH1/2/3}$ range, V_{DD} falls outside of a valid $V_{DD1/2/3/4}$ range, or #RESET ≠ V_{IH} or V_{HH}. If V_{PP} error is detected, status register bit SR.3 is set to "1" along with SR.4 or SR.5, depending on the attempted operation. If #RESET

transitions to V_{IL} during block erase or word/byte write, RY/#BY will remain low until the reset operation is complete. Then, the operation will abort and the device will enter deep power-down. The aborted operation may leave data partially altered. Therefore, the command sequence must be repeated after normal operation is restored. Device power-off or #RESET transitions to V_{IL} clear the status register.

The CUI latches commands issued by system software and is not altered by V_{PP} or #CE transitions or WSM actions. Its state is read array mode upon power-up, after exit from deep power-down or after V_{DD} transitions below V_{LKO}.

After block erase or word/byte write, even after V_{PP} transitions down to V_{PPLK}, the CUI must be placed in read array mode via the Read Array command if subsequent access to the memory array is desired.

Power-up/Down Protection

The device is designed to offer protection against accidental block erasure or word/byte writing during power transitions. Upon power-up, the device is indifferent as to which power supply (V_{PP} or V_{DD}) powers-up first. Internal circuitry resets the CUI to read array mode at power-up. A system designer must guard against spurious writes for V_{DD} voltages above V_{LKO} when V_{PP} is active. Since both #WE and #CE must be low for a command write, driving either to V_{IH} will inhibit writes. The CUI's two-step command sequence architecture provides added level of protection against data alteration.

#WP provide additional protection from inadvertent code or data alteration. The device is disabled while #RESET = V_{IL} regardless of its control inputs state.

Power Dissipation

When designing portable systems, designers must consider battery power consumption not only during device operation, but also for data retention during system idle time. Flash memory's non-volatility increases usable battery life because data is retained when system power is removed.

In addition, deep power-down mode ensures extremely low power consumption even when system power is applied. For example, portable computing products and other power sensitive applications that use an array of devices for solid-state storage can consume negligible power by lowering #RESET to V_{IL} standby or sleep modes. If access is again needed, the devices can be read following the t_{PHQV} and t_{PHWL} wake-up cycles required after #RESET is first raised to V_{IH}. See AC Characteristics - Read Only and Write Operations and Figures 13, 14, 15 and 16 for more information.

11. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings*

Operating Temperature
During Read, Block Erase, and Word/Byte Write ..... 0° C to +70° C (1)
Temperature under Bias ..... -10° C to +80° C

Storage Temperature ..... –65° C to +125° C

Voltage On Any Pin
(except V_{DD}, V_{PP} and #RESET) ..... -0.5V to +7.0V (2)

V_{DD} Supply Voltage..... -0.2V to +7.0V (2)

V_{PP} Update Voltage during Block
Erase and Word/Byte Write ..... -0.2V to +14.0V (2, 3)

#RESET Voltage ..... -0.5V to +14.0V (2, 3)

Output Short Circuit Current .....100 mA (4)

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

Notes:

1. Operating temperature is for commercial temperature product defined by this specification.
2. All specified voltages are with respect to V_{SS}. Minimum DC voltage is -0.5V on input/output pins and -0.2V on V_{DD} and V_{PP} pins. During transitions, this level may undershoot to -2.0V for periods <20 nS. Maximum DC voltage on input/output pins and V_{DD} is V_{DD} +0.5V which, during transitions, may overshoot to V_{DD} +2.0V for periods <20 nS.
3. Maximum DC voltage on V_{PP} and #RESET may overshoot to +14.0V for periods <20 nS.
4. Output shorted for no more than one second. No more than one output shorted at a time.

Operating Conditions

Temperature and V_{DD} Operating Conditions

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	TEST CONDITION
Operating Temperature	T_A	0	+70	°C	Ambient Temperature
V_{DD} Supply Voltage (2.7V to 3.6V)	V_{DD1}	2.7	3.6	V	
V_{DD} Supply Voltage (3.3V ±0.3V)	V_{DD2}	3.0	3.6	V	
V_{DD} Supply Voltage (5.0V ±0.25V)	V_{DD3}	4.75	5.25	V	
V_{DD} Supply Voltage (5.0V ±0.5V)	V_{DD4}	4.50	5.50	V	

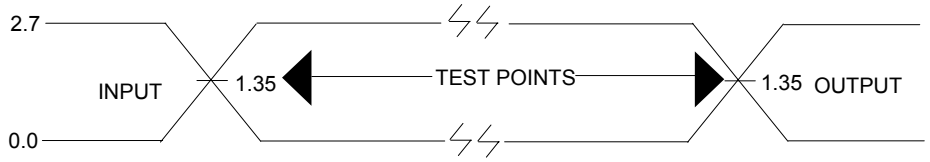
Capacitance(1)

T_A = +25° C, f = 1 MHz

PARAMETER	SYMBOL	TYP.	MAX.	UNIT	CONDITION
Input Capacitance	C_{IN}	7	10	pF	V_{IN} = 0.0V
Output Capacitance	C_{OUT}	9	12	pF	V_{OUT} = 0.0V

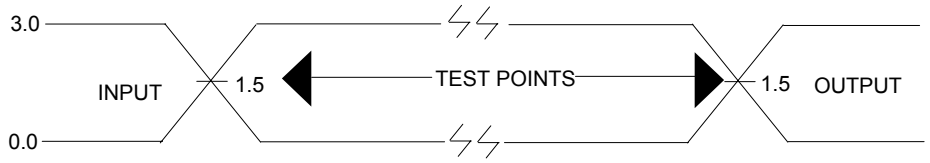
Note: Sampled, not 100% tested.

AC Input/Output Test Conditions



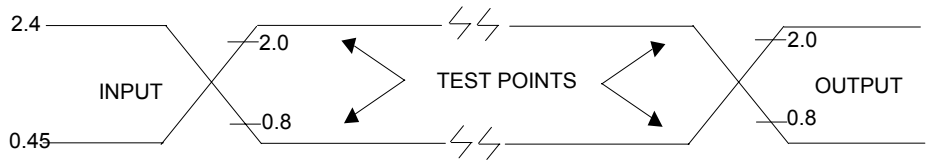
AC test inputs are driven at 2.7V for a Logic "1" and 0.0V for a Logic "0". Input timing begins, and output timing ends, at 1.35V. Input rise and fall times (10% to 90%) <10 nS.

Figure 9. Transient Input/Output Reference Waveform for V_{DD} = 2.7V to 3.6V



AC test inputs are driven at 3.0V for a Logic "1" and 0.0V for a Logic "0". Input timing begins, and output timing ends, at 1.5V. Input rise and fall times (10% to 90%) <10 nS.

Figure 10. Transient Input/Output Reference Waveform for V_{DD} = 3.3V ±0.3V and V_{DD} = 5V ±0.25V (High Speed Testing Configuration)



AC test inputs are driven at V_{OH} (2.4 V_{TTL}) for a Logic "1" and V_{OL} (0.45 V_{TTL}) for a Logic "0." Input timing begins at V_{IH} (2.0 V_{TTL}) and V_{IL} (0.8 V_{TTL}). Output timing ends at V_{IH} and V_{IL}. Input rise and fall times (10% to 90%) <10 nS.

Figure 11. Transient Input/Output Reference Waveform for V_{DD} = 5V ±0.5V (Standard Testing Configuration)

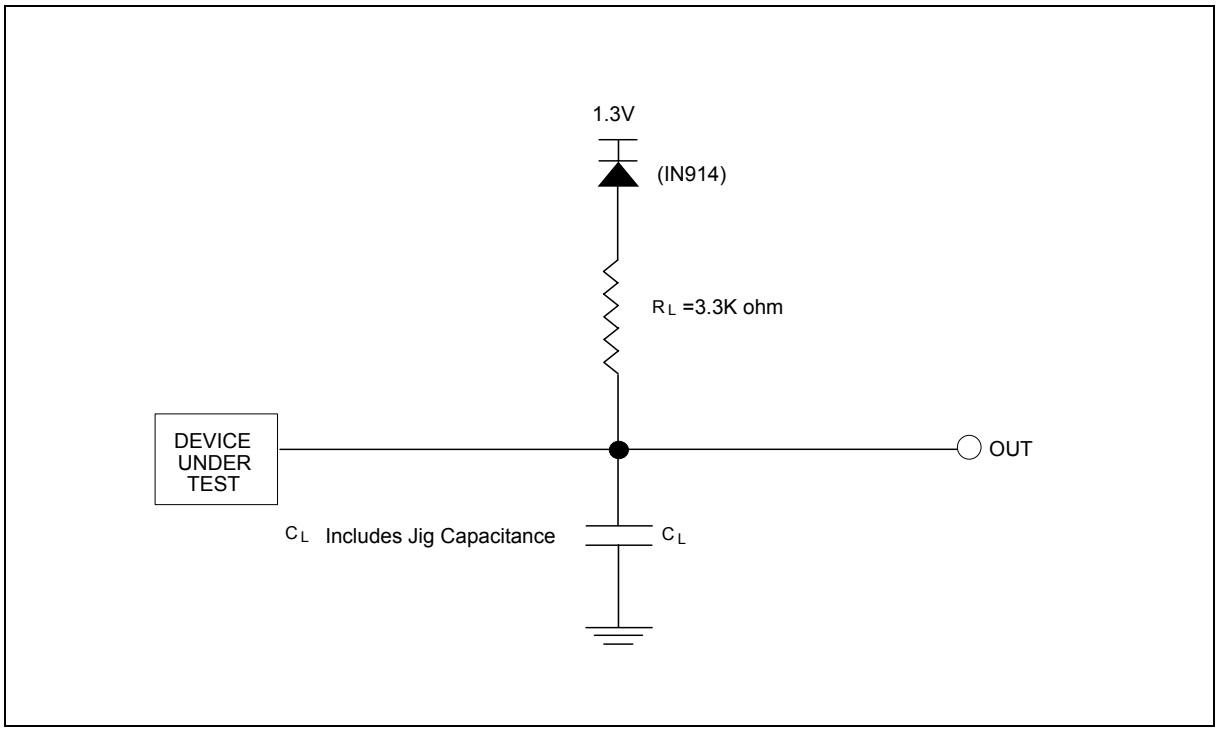


Figure 12. Transient Equivalent Testing Load Circuit

Test Configuration Capacitance Loading Value

TEST CONFIGURATION	CL(PF)
V_{DD} = 3.3V ±0.3V, 2.7V to 3.6V	30
V_{DD} = 5V ±0.25V	30
V_{DD} = 5V ±0.5V	100

DC Characteristics

PARAMETER	SYM.	TEST CONDITIONS	V_{DD} = 2.7V– 3.6V		V_{DD} = 5V ±0.5		UNIT
			Typ.	Max.	Typ.	Max.	
Input Load Current (Note1)	I_{LI}	V_{DD} = V_{DD} Max. V_{IN} = V_{DD} or V_{SS}		±0.5		±1	µA
Output Leakage Current (Note1)	I_{LO}	V_{DD} = V_{DD} Max. V_{OUT} = V_{DD} or V_{SS}		±0.5		±10	µA
V_{DD} Standby Current (Note 1, 3, 6, 10)	I_{CCS}	CMOS Level Inputs V_{DD} = V_{DD} Max. #CE = #RESET = V_{DD} ±0.2V	25	50	30	100	µA
		TTL Level Inputs V_{DD} = V_{DD} Max. #CE = #RESET = V_{IH}	0.2	2	0.4	2	mA
V_{DD} Reset Power-down Current (Note 1, 10)	I_{CCD}	#RESET = V_{SS} ±0.2V I_{OUT}(RY/#BY) = 0 mA	4	10		10	µA

V_{DD} Read Current (Note 1, 5, 6)	I_{CCR}	CMOS Inputs
		V_{DD} = V_{DD} Max., #CE = V_{SS},
		f = 5 MHz (3.3V ±0.3),
		f = 5 MHz (2.7V – 3.6V)
		f = 8 MHz (5V± 0.5V)
		IOUT = 0 mA
			15	25		50	mA

		TTL Inputs
		V_{DD} = V_{DD} Max., #CE = V_{SS},
		f = 5 MHz (3.3V ±0.3),
		f = 5 MHz (2.7V – 3.6V)
		f = 8 MHz (5V ±0.5V), IOUT = 0 mA
				30		65	mA

V_{DD} Word/Byte Write Current (Note 1, 7)	I_{CCW}	V_{PP} = 2.7V – 3.6V	5	17	-	-	mA
		V_{PP} = 4.5V – 5.5V	5	17		35	mA
		V_{PP} = 11.4V – 12.6V	5	12		30	mA
V_{DD} Block Erase Current (Note 1, 7)	I_{CCE}	V_{PP} = 2.7V – 3.6V	4	17	-	-	mA
		V_{PP} = 4.5V – 5.5V	4	17		30	mA
		V_{PP} = 11.4V – 12.6V	4	12		25	mA
V_{DD} Word/Byte Write or Block Erase Suspend Current (Note1, 2)	I_{CCWS} I_{CCES}	#CE = V_{IH}	1	6	1	10	mA
V_{PP} Standby or Read Current (Note1)	I_{PPS}	$V_{PP} \le V_{DD}$	±2	±15	±2	±15	µA
	I_{CPPR}	$V_{PP} > V_{DD}$	10	200	10	200	µA
V_{PP} Deep Power-Down Current (Note1)	I_{PPD}	#RESET = V_{SS} ±0.2V	0.1	5	0.1	5	µA
V_{PP} Word/Byte Write Current (Note 1, 7)	I_{PPW}	V_{PP} = 2.7V – 3.6V	12	40	-	-	mA
		V_{PP} = 4.5V – 5.5V		40		40	mA
		V_{PP} = 11.4V – 12.6V		30		30	mA
V_{PP} Block Erase Current (Note 1, 7)	I_{PPE}	V_{PP} = 2.7V – 3.6V	8	25	-	-	mA
		V_{PP} = 4.5V – 5.5V		25		25	mA
		V_{PP} = 11.4V – 12.6V		20		20	mA
V_{PP} Word/Byte Write or Block Erase Suspend Current (Note 1)	I_{PPWS} I_{PPES}	V_{PP} = $V_{PPH1/2/3}$	10	200	10	200	µA

DC Characteristics (Continued)

PARAMETER	SYM.	TEST CONDITIONS	V_{DD} = 2.7V - 3.6V		V_{DD} = 5V ±0.5V		UNIT
			Min.	Max.	Min.	Max.	
Input Low Voltage (Note 7)	V_{IL}		-0.5	0.8	-0.5	0.8	V
Input High Voltage (Note 7)	V_{IH}		2.0	V_{DD} +0.5	2.0	V_{DD} +0.5	V
Output Low Voltage (Note 3, 7)	V_{OL}	V_{DD} = V_{DD} Min. I_{OL} = 5.8 mA (5V ±0.5V) I_{OL} = 2.0 mA (3.3V ±0.3V) I_{OL} = 2.0 mA (2.7V – 3.6V)		0.4		0.45	V
Output High Voltage (TTL) (Note 3, 7)	V_{OH1}	V_{DD} = V_{DD} Min. I_{OH} = -2.5 mA (5V ±0.5V) I_{OH} = -2.0 mA (3.3V ±0.3V) I_{OH} = -1.5 mA (2.7V – 3.6V)	2.4		2.4		V
Output High Voltage (CMOS) (Note 3, 7)	V_{OH2}	V_{DD} = V_{DD} Min. I_{OH} = -2.0 mA	0.85 V_{DD}		0.85 V_{DD}		V
			V_{DD} -0.4		V_{DD} -0.4		V
V_{PP} Lockout during Normal Operations (Note 4, 7)	V_{PPLK}	V_{DD} = V_{DD} Min. I_{OH} = -100 µA		1.5		1.5	V
V_{PP} during Block Erase or Word/Byte Write Operations	V_{PPH1}		2.7	3.6	-	-	V
V_{PP} during Block Erase or Word/Byte Write Operations	V_{PPH2}		4.5	5.5	4.5	5.5	V
V_{PP} during Block Erase or Word/Byte Write Operations	V_{PPH3}		11.4	12.6	11.4	12.6	V
V_{DD} Lockout Voltage	V_{LKO}		2.0		2.0		V
#RESET Unlock Voltage (Note 8, 9)	V_{HH}	Unavailable #WP	11.4	12.6	11.4	12.6	V

Notes:

1. All currents are in RMS unless otherwise noted. Typical values at nominal V_{DD} voltage and T_A = +25° C.
2. I_{CCWS} and I_{CCES} are specified with the device de-selected. If read or word/byte written while in erase suspend mode, the device's current draw is the sum of I_{CCWS} or I_{CCES} and I_{CCR} or I_{CCW}, respectively.
3. Includes RY/#BY.
4. Block erases and word/byte writes are inhibited when $V_{PP} \le V_{PPLK}$, and not guaranteed in the range between V_{PPLK} (max.) and V_{PPH1} (min.), between V_{PPH1} (max.) and V_{PPH2} (min.), between V_{PPH2} (max.) and V_{PPH3} (min.), and above V_{PPH3} (max.).
5. Automatic Power Savings (APS) reduces typical I_{CCR} to 1mA at 5V V_{DD} and 3 mA at 2.7V and 3.3V V_{DD} in static operation.
6. CMOS inputs are either V_{DD} ±0.2V or V_{SS} ±0.2V. TTL inputs are either V_{IL} or V_{IH}.
7. Sampled, not 100% tested.
8. Boot block erases and word/byte writes are inhibited when the corresponding #RESET = V_{IH} and #WP = V_{IL}. Block erase and word/byte write operations are not guaranteed with V_{IH} < #RESET < V_{HH} and should not be attempted.
9. #RESET connection to a V_{HH} supply is allowed for a maximum cumulative period of 80 hours.
10. #BYTE input level is V_{DD} ±0.2V in word mode or V_{SS} ±0.2V in byte mode. #WP input level is V_{DD} ±0.2V or V_{SS} ±0.2V.

AC Characteristics - Read-only Operations(1)

V_{DD} = 2.7V to 3.6V, T_A = 0° C to +70° C

PARAMETER	SYM.	MIN.	MAX.	UNIT
Read Cycle Time	t_{AVAV}	120		nS
Address to Output Delay	t_{AVQV}		120	nS
#CE to Output Delay (Note 2)	t_{ELQV}		120	nS
#RESET High to Output Delay	t_{PHQV}		600	nS
#OE to Output Delay (Note 2)	t_{GLQV}		50	nS
#CE to Output in Low Z (Note 3)	t_{ELQX}	0		nS
#CE High to Output in High Z (Note 3)	t_{EHQZ}		55	nS
#OE to Output in Low Z (Note 3)	t_{GLQX}	0		nS
#OE High to Output in High Z (Note 3)	t_{GHQZ}		20	nS
Output Hold from Address –, #CE or #OE Change, Whichever Occurs First (Note 3)	t_{OH}	0		nS
#BYTE to Output Delay (Note 3)	t_{FVQV}		120	nS
#BYTE Low to Output in High Z (Note 3)	t_{FLQZ}		30	nS
#CE to #BYTE High or Low (Note 3, 6)	t_{ELFV}		5	nS

Notes: See 5.0V V_{DD} Read-only Operations for notes 1 through 6.

V_{DD} = 3.3V ±0.3V, T_A = 0 ° C to +70° C

PARAMETER	SYM.	MIN.	MAX.	UNIT
Read Cycle Time	t_{AVAV}	100		nS
Address to Output Delay	t_{AVQV}		100	nS
#CE to Output Delay (Note 2)	t_{ELQV}		100	nS
#RESET High to Output Delay	t_{PHQV}		600	nS
#OE to Output Delay (Note 2)	t_{GLQV}		50	nS
#CE to Output in Low Z (Note 3)	t_{ELQX}	0		nS
#CE High to Output in High Z (Note 3)	t_{EHQZ}		55	nS
#OE to Output in Low Z (Note 3)	t_{GLQX}	0		nS
#OE High to Output in High Z (Note 3)	t_{GHQZ}		20	nS
Output Hold from Address, #CE or #OE Change, Whichever Occurs First (Note 3)	t_{OH}	0		nS
#BYTE to Output Delay (Note 3)	t_{FVQV}		100	nS
#BYTE Low to Output in High Z (Note 3)	t_{FLQZ}		30	nS
#CE to #BYTE High or Low (Note 3, 6)	t_{ELFV}		5	nS

Note: See 5.0V V_{DD} Read-only Operations for notes 1 through 6.

V_{DD} = 5V ±0.5V, 5V ±0.25V, T_A = 0 ° C to +70° C

PARAMETER	SYM.	V_{DD} = 5V ±0.25V(4)		5V ±0.5V(5)		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{AVAV}	85		90		nS
Address to Output Delay	t_{AVQV}		85		90	nS
#CE to Output Delay (Note 2)	t_{ELQV}		85		90	nS
#RESET High to Output Delay	t_{PHQV}		400		400	nS
#OE to Output Delay (Note 2)	t_{GLQV}		40		45	nS
#CE to Output in Low Z (Note 3)	t_{ELQX}	0		0		nS
#CE High to Output in High Z (Note 3)	t_{EHQZ}		55		55	nS
#OE to Output in Low Z (Note 3)	t_{GLQX}	0		0		nS
#OE High to Output in High Z (Note 3)	t_{GHQZ}		10		10	nS
Output Hold from Address, #CE or #OE Change, Whichever Occurs First (Note 3)	t_{OH}	0				nS
#BYTE to Output Delay (note3)	t_{FVQV}		85		90	nS
#BYTE Low to Output in High Z (Note 3)	t_{FLQZ}		25		30	nS
#CE to #BYTE High or Low (Note 3, 6)	t_{ELFV}		5		5	nS

Notes:

1. See AC Input/Output Reference Waveform for maximum allowable input slew rate.
2. #OE may be delayed up to t_{ELQV} to t_{GLQV} after the falling edge of #CE without impact on t_{ELQV}.
3. Sampled, not 100% tested.
4. See Transient Input/Output Reference Waveform and Transient Equivalent Testing Load Circuit (High Speed Configuration) for testing characteristics.
5. See Transient Input/Output Reference Waveform and Transient Equivalent Testing Load Circuit (Standard Configuration) for testing characteristics.
6. If #BYTE transfer during reading cycle, exist the regulations separately.

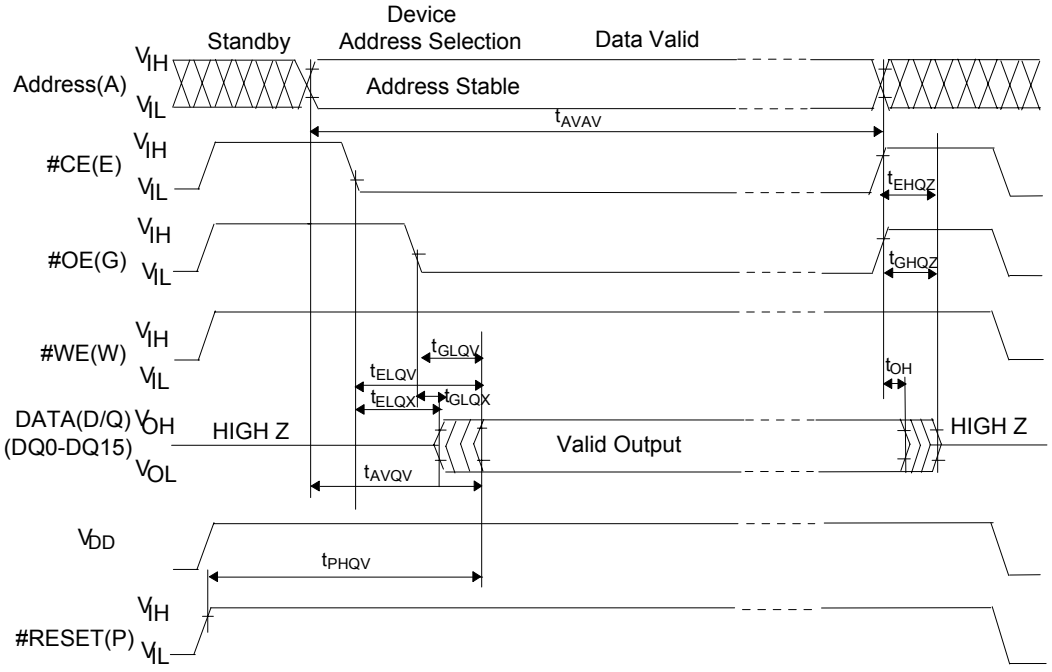


Figure 13. AC Waveform for Read Operations

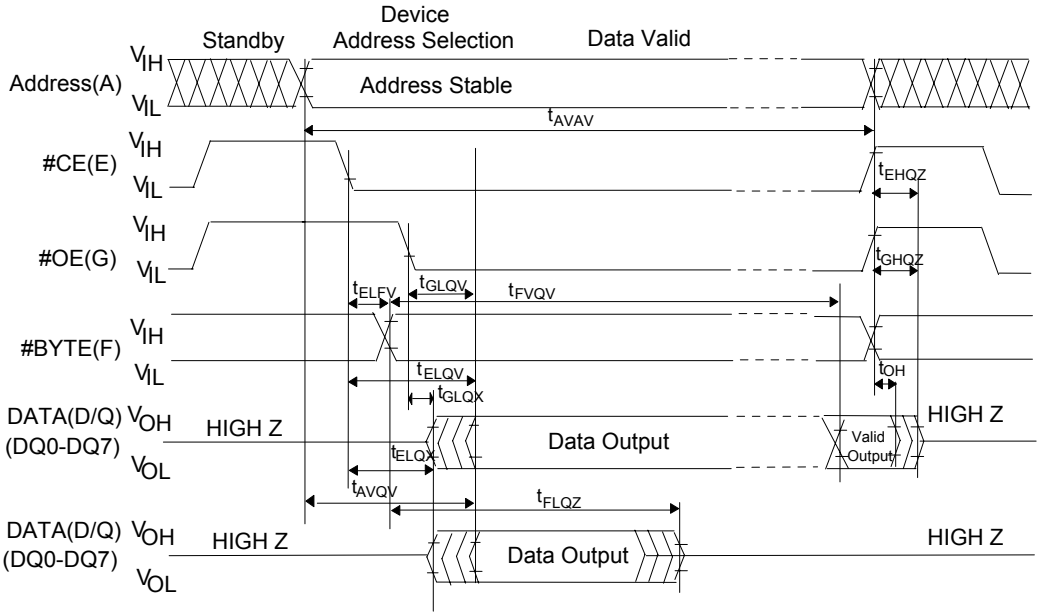


Figure 14. #BYTE Timing Waveform

AC Characteristics - Write Operations(1)

V_{DD} = 2.7V to 3.6V, T_A = 0° C to +70° C

PARAMETER	SYM.	MIN.	MAX.	UNIT
Write Cycle Time	t_{AVAV}	120		nS
#RESET High Recovery to #WE Going Low (Note 2)	t_{PHWL}	1		µS
#CE Setup to #WE Going Low	t_{ELWL}	10		nS
#WE Pulse Width	t_{WLWH}	50		nS
#RESET V_{HH} Setup to #WE Going High (Note 2)	T_{PHHWH}	100		nS
#WP V_{IH} Setup to #WE Going High (Note 2)	t_{SHWH}	100		nS
V_{PP} Setup to #WE Going High (Note 2)	t_{VPWH}	100		nS
Address Setup to #WE Going High (Note 3)	t_{AVWH}	50		nS
Data Setup to #WE Going High (Note 3)	t_{DVWH}	50		nS
Data Hold from #WE High	t_{WHDX}	0		nS
Address Hold from #WE High	t_{WHAX}	5		nS
#CE Hold from #WE High	t_{WHEH}	10		nS
#WE Pulse Width High	t_{WHWL}	30		nS
#WE High to RY/#BY Going Low	t_{WHRL}		100	nS
Write Recovery before Read	t_{WHGL}	0		nS
V_{PP} Hold from Valid SRD, RY/#BY High (Note 2, 4)	t_{QVVL}	0		nS
#RESET V_{HH} Hold from Valid (Note 2, 4)	T_{QVPH}	0		nS
#WP V_{IH} Hold from Valid SRD, RY/#BY High (Note 2, 4)	t_{QVSL}	0		nS
#BYTE Setup to #WE Going High (Note 7)	t_{FVWH}	50		nS
#BYTE Hold from #WE High (Note 7)	t_{WHFV}	120		nS

Note: See 5.0V V_{DD} AC Characteristics - Write Operations for notes 1 through 7.

V_{DD} = 3.3V ±0.3V, T_A = 0 ° C to +70° C

PARAMETER	SYM.	MIN.	MAX.	UNIT
Write Cycle Time	t_{AVAV}	100		nS
#RESET High Recovery to #WE Going Low (Note 2)	t_{PHWL}	1		µS
#CE Setup to #WE Going Low	t_{ELWL}	10		nS
#WE Pulse Width	t_{WLWH}	50		nS
#RESET V_{HH} Setup to #WE Going High (Note 2)	T_{PHHWH}	100		nS
#WP V_{IH} Setup to #WE Going High (Note 2)	t_{SHWH}	100		nS
V_{PP} Setup to #WE Going High (Note 2)	t_{VPWH}	100		nS
Address Setup to #WE Going High (Note 3)	t_{AVWH}	50		nS
Data Setup to #WE Going High (Note 3)	t_{DVWH}	50		nS
Data Hold from #WE High	t_{WHDX}	0		nS
Address Hold from #WE High	t_{WHAX}	5		nS
#CE Hold from #WE High	t_{WHEH}	10		nS
#WE Pulse Width High	t_{WHWL}	30		nS
#WE High to RY/#BY Going Low	t_{WHRL}		100	nS
Write Recovery before Read	t_{WHGL}	0		nS
V_{PP} Hold from Valid SRD, RY/#BY High (Note 2, 4)	t_{QVVL}	0		nS
#RESET V_{HH} Hold from Valid (Note 2, 4)	T_{QVPH}	0		nS
#WP V_{IH} Hold from Valid SRD, RY/#BY High (Note 2, 4)	t_{QVSL}	0		nS
#BYTE Setup to #WE Going High (Note 7)	t_{FVWH}	50		nS
#BYTE Hold from #WE High (Note 7)	t_{WHFV}	100		nS

Note: See 5.0V V_{DD} AC Characteristics - Write Operations for notes 1 through 7.

V_{DD} = 5V ±0.5V, 5V ±0.25V, T_A = 0 ° C to +70° C

PARAMETER	SYM.	5V ±0.25V(5)		5V ±0.5V(6)		UNIT
		MIN.	MAX.	MIN	MAX.	
Write Cycle Time	t_{AVAV}	85		90		nS
#RESET High Recovery to #WE Going Low (Note 2)	t_{PHWL}	1		1		µS
#CE Setup to #WE Going Low	t_{ELWL}	10		10		nS
#WE Pulse Width	t_{WLWH}	40		40		nS
#RESET V_{HH} Setup to #WE Going High (Note 2)	T_{PHHWH}	100		100		nS
#WP V_{IH} Setup to #WE Going High (Note 2)	t_{SHWH}	100		100		nS
V_{PP} Setup to #WE Going High (Note 2)	t_{VPWH}	100		100		nS
Address Setup to #WE Going High (Note 3)	t_{AVWH}	40		40		nS
Data Setup to #WE Going High (Note 3)	t_{DVWH}	40		40		nS
Data Hold from #WE High	t_{WHDX}	0		0		nS
Address Hold from #WE High	t_{WHAX}	5		5		nS
#CE Hold from #WE High	t_{WHEH}	10		10		nS
#WE Pulse Width High	t_{WHWL}	30		30		nS
#WE High to RY/#BY Going Low	t_{WHRL}		90		90	nS
Write Recovery before Read	t_{WHGL}	0		0		nS
V_{PP} Hold from Valid SRD, RY/#BY High (Note 2, 4)	t_{QVVL}	0		0		nS
#RESET V_{HH} Hold from Valid SRD, RY/BY# High (Note 2, 4)	T_{QVPH}	0		0		
#WP V_{IH} Hold from Valid SRD, RY/#BY High (Note 2, 4)	t_{QVSL}	0		0		nS
#BYTE Setup to #WE Going High (Note 7)	t_{FVWH}	40		40		nS
#BYTE Hold from #WE High (Note 7)	t_{WHFV}	85		90		nS

Notes:

1. Read timing characteristics during block erase and word/byte write operations are the same as during read-only operations. Refer to AC Characteristics for read-only operations.
2. Sampled, not 100% tested.
3. Refer to Table 4 for valid AIN and DIN for block erase or word/byte write.
4. V_{PP} should be held at $V_{PPH1/2/3}$ (and if necessary #RESET should be held at V_{HH}) until determination of block erase or word/byte write success (SR.1/3/4/5 = 0).
5. See Transient Input/Output Reference Waveform and Transient Equivalent Testing Load Circuit (High Seed Configuration) for testing characteristics.
6. See Transient Input/Output Reference Waveform and Transient Equivalent Testing Load Circuit (Standard Configuration) for testing characteristics.
7. If #BYTE switch during reading cycle, exist the regulations separately.

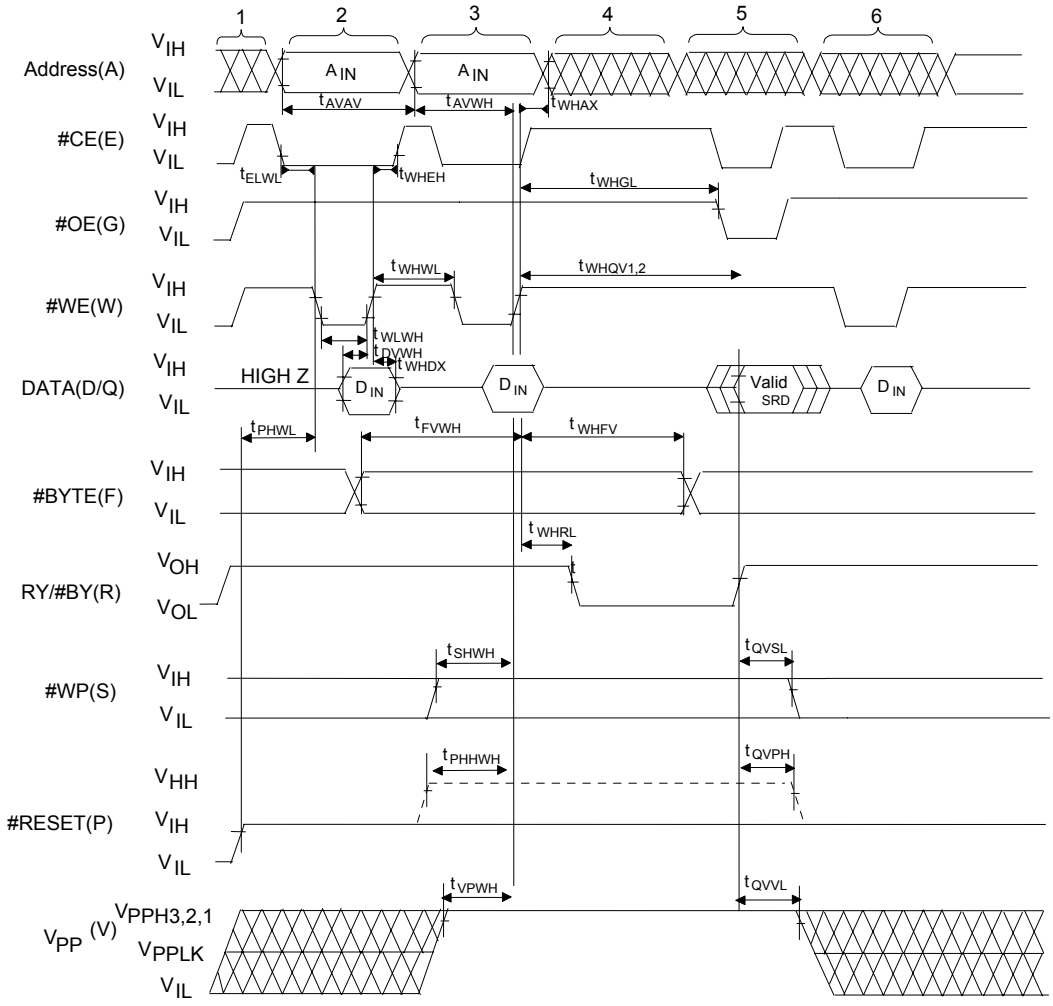


Figure 15. AC Waveform for #WE-Controlled Write Operations

Notes:

1. V_{DD} power-up and standby.
2. Write block erase or word/byte write setup.
3. Write block erase confirm or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. Write Read Array command.

Alternative #CE-Controlled Writes(1)

V_{DD} = 2.7V to 3.6V, T_A = 0° C to +70° C

PARAMETER	SYM.	MIN.	MAX.	UNIT
Write Cycle Time	t_{AVAV}	120		nS
#RESET High Recovery to #CE Going Low (Note 2)	t_{PHEL}	1		µS
#WE Setup to #CE Going Low	t_{WLEL}	0		nS
#CE Pulse Width	t_{ELEH}	70		nS
#RESET V_{HH} Setup to #CE Going High (Note 2)	t_{PHHEH}	100		nS
#WP V_{IH} Setup to #CE Going High (Note 2)	t_{SHEH}	100		nS
V_{PP} Setup to #CE Going High (Note 2)	t_{VPEH}	100		nS
Address Setup to #CE Going High (Note 3)	t_{AVEH}	50		nS
Data Setup to #CE Going High (Note 3)	t_{DVEH}	50		nS
Data Hold from #CE High	t_{EHDX}	0		nS
Address Hold from #CE High	t_{EHAX}	5		nS
#WE Hold from #CE High	t_{EHWH}	0		nS
#CE Pulse Width High	t_{EHEL}	25		nS
#CE High to RY/#BY Going Low	t_{EHRL}		100	nS
Write Recovery before Read	t_{EHGL}	0		nS
V_{PP} Hold from Valid SRD, RY/#BY High (Note 2, 4)	t_{QVVL}	0		nS
#RESET V_{HH} Hold from Valid SRD, RY/#BY High (Note 2, 4)	T_{QVPH}	0		nS
#WP V_{IH} Hold from Valid SRD, RY/#BY High (Note 2, 4)	t_{QVSL}	0		nS
#BYTE Setup to #CE Going High (Note 7)	t_{FVEH}	50		nS
#BYTE Hold from #CE High (Note 7)	t_{EHFV}	120		nS

Note: See 5.0V V_{DD} Alternative #CE-Controlled Writes for notes 1 through 7.

V_{DD} = 3.3V ±0.3V, T_A = 0 ° C to +70° C

PARAMETER	SYM.	MIN.	MAX.	UNIT
Write Cycle Time	t_{AVAV}	100		nS
#RESET High Recovery to #CE Going Low (Note 2)	t_{PHEL}	1		µS
#WE Setup to #CE Going Low	t_{WLEL}	0		nS
#CE Pulse Width	t_{ELEH}	70		nS
#RESET V_{HH} Setup to #CE Going High (Note 2)	t_{PHHEH}	100		nS
#WP V_{IH} Setup to #CE Going High (Note 2)	t_{SHEH}	100		nS
V_{PP} Setup to #CE Going High (Note2)	t_{VPEH}	100		nS
Address Setup to #CE Going High (Note 3)	t_{AVEH}	50		nS
Data Setup to #CE Going High (Note 3)	t_{DVEH}	50		nS
Data Hold from #CE High	t_{EHDX}	0		nS
Address Hold from #CE High	t_{EHAX}	5		nS
#WE Hold from #CE High	t_{EHWH}	0		nS
#CE Pulse Width High	t_{EHEL}	25		nS
#CE High to RY/#BY Going Low	t_{EHRL}		100	nS
Write Recovery before Read	t_{EHGL}	0		nS
V_{PP} Hold from Valid SRD, RY/#BY High (Note 2, 4)	t_{QVVL}	0		nS
#RESET V_{HH} Hold from Valid SRD, RY/#BY High (Note 2, 4)	T_{QVPH}	0		nS
#WP V_{IH} Hold from Valid SRD, RY/#BY High (Note 2, 4)	t_{QVSL}	0		nS
#BYTE Setup to #CE Going High (Note 7)	t_{FVEH}	50		nS
#BYTE Hold from #CE High (Note 7)	t_{EHFV}	100		nS

Note: See 5.0V V_{DD} Alternative #CE-Controlled Writes for notes 1 through 7.

V_{DD} = 5V ±0.5V, 5V ±0.25V, T_A = 0 ° C to +70° C

PARAMETER	SYM.	V_{DD} = 5V ±0.25V(5)		5V ±0.5V(6)		UNIT
		Min.	Max.	Min.	Max.	
Write Cycle Time	t_{AVAV}	85		90		nS
#RESET High Recovery to #CE Going Low (Note 2)	t_{PHEL}	1		1		µS
#WE Setup to #CE Going Low	t_{WLEL}	0		0		nS
#CE Pulse Width	t_{ELEH}	50		50		nS
#RESET V_{HH} Setup to #CE Going High (Note 2)	t_{PHHEH}	100		100		nS
#WP V_{IH} Setup to #CE Going High (Note 2)	t_{SHEH}	100		100		nS
V_{PP} Setup to #CE Going High (Note 2)	t_{VPEH}	100		100		nS
Address Setup to #CE Going High (Note 3)	t_{AVEH}	40		40		nS
Data Setup to #CE Going High (Note 3)	t_{DVEH}	40		40		nS
Data Hold from #CE High	t_{EHDX}	0		0		nS
Address Hold from #CE High	t_{EHAX}	5		5		nS
#WE Hold from #CE High	t_{EHWH}	0		0		nS
#CE Pulse Width High	t_{EHEL}	25		25		nS
#CE High to RY/#BY Going Low	t_{EHRL}		90		90	nS
Write Recovery before Read	t_{EHGL}	0		0		nS
V_{PP} Hold from Valid SRD, RY/#BY High (Note 2, 4)	t_{QVVL}	0		0		nS
#RESET V_{HH} Hold from Valid SRD, RY/#BY High (Note 2, 4)	T_{QVPH}	0		0		nS
#WP V_{IH} Hold from Valid SRD, RY/#BY High (Note 2, 4)	t_{QVSL}	0		0		nS
#BYTE Setup to #CE Going High (Note 7)	t_{FVEH}	40		40		nS
#BYTE Hold from #CE High (Note 7)	t_{EHFV}	85		90		nS

Notes:

1. In systems where #CE defines the write pulse width (within a longer #WE timing waveform), all setup, hold, and inactive #WE times should be measured relative to the #CE waveform.
2. Sampled, not 100% tested.
3. Refer to Table 4 for valid AIN and DIN for block erase or word/byte write.
4. V_{PP} should be held at $V_{PPH1/2/3}$ (and if necessary #RESET should be held at V_{HH}) until determination of block erase or word/byte write success (SR.1/3/4/5 = 0).
5. See Transient Input/Output Reference Waveform and Transient Equivalent Testing Load Circuit (High Seed Configuration) for testing characteristics.
6. See Transient Input/Output Reference Waveform and Transient Equivalent Testing Load Circuit (Standard Configuration) for testing characteristics.
7. If #BYTE switch during reading cycle, exist the regulations separately.

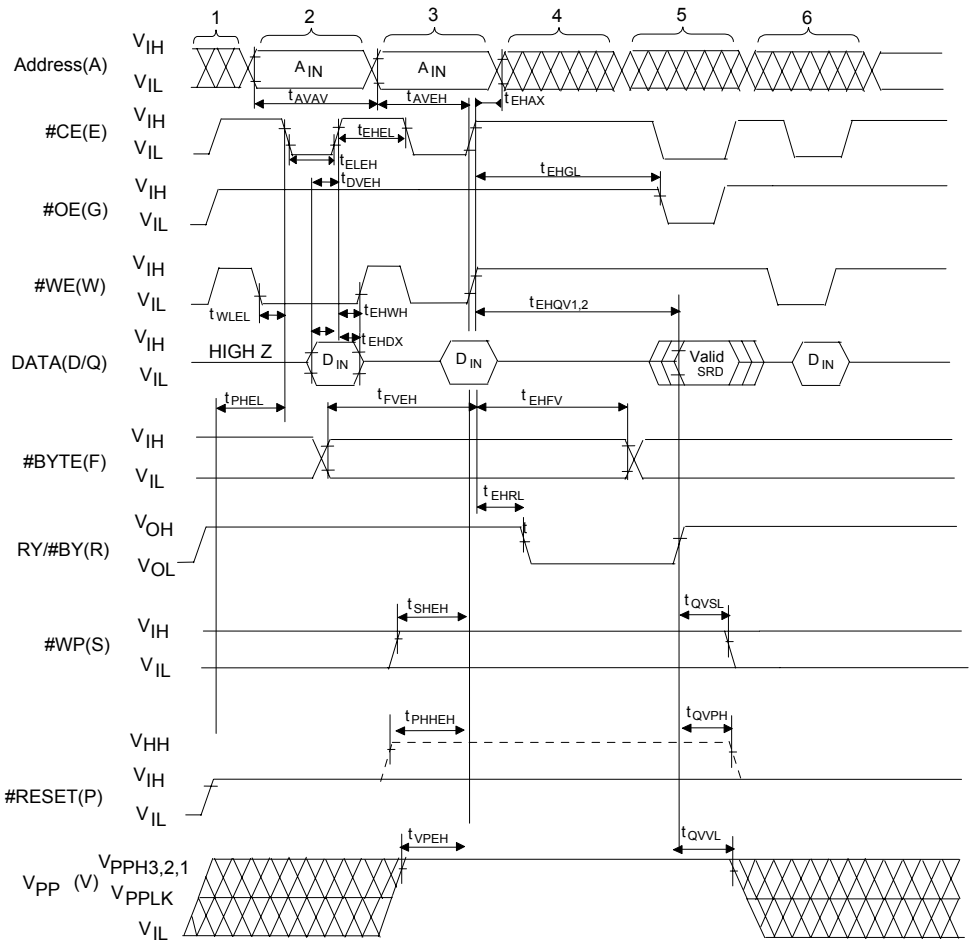


Figure 16. AC Waveform for #CE-Controlled Write Operations

Notes:

1. V_{DD} power-up and standby.
2. Write block erase or word/byte write setup.
3. Write block erase confirm or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. Write Read Array command.

Reset Operations

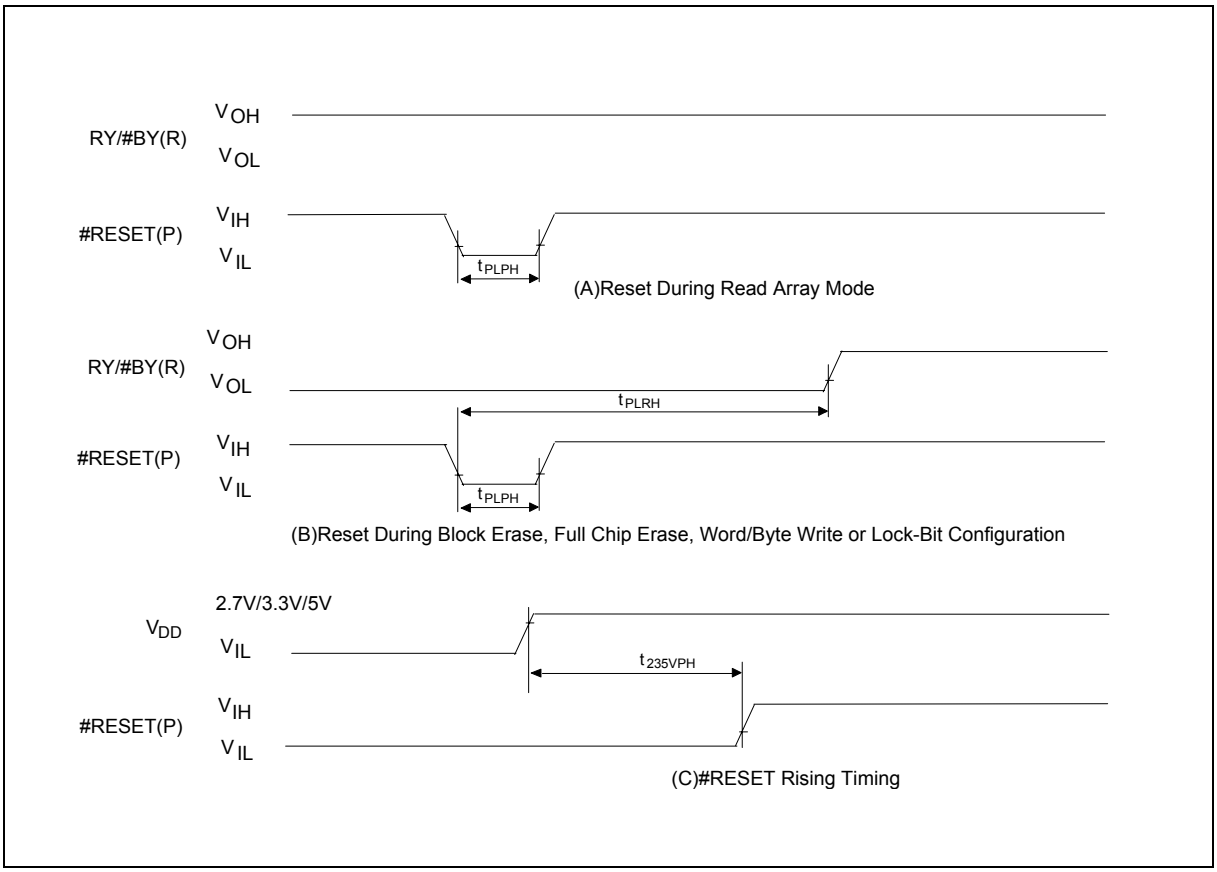


Figure 17. AC Waveform for Reset Operation

Reset AC Specifications

SYM.	PARAMETER	V_{DD} = 2.7V – 3.6V		V_{DD} = 3.0V – 3.6V		V_{DD} = 4.5V – 5.5V		UNIT
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLPH}	#RESET Pulse Low Time (If RP# is tied to V_{DD}, this specification is not applicable)	100		100		100		nS
t_{PLRH}	#RESET Low to Reset during Block Erase or Word/Byte Write (Note 1, 2)		22		20		12	μS
t_{235VPH}	V_{DD} 2.7V to #RESET High V_{DD} 3.0V to #RESET High V_{DD} 4.5V to #RESET High (Note 3)	100		100		100		nS

Notes:

1. If #RESET is asserted while a block erase or word/byte write operation is not executing, the reset will complete within 100nS.
2. A reset time, t_{PHQV}, is required from the later of RY/#BY or #RESET going high until outputs are valid.
3. When the device power-up, holding #RESET low minimum 100 nS is required after V_{DD} has been in predefined range and also has been in stable there.

Block Erase And Word/Byte Write Performance(3)

V_{DD} = 2.7V to 3.6V, T_A = 0° C to +70° C

SYM.	PARAMETER		NOTE	V_{PP} = 2.7V – 3.6V		V_{PP} = 4.5V – 5.5V		V_{PP} = 11.4V – 12.6V		UNIT
				TYP.(1)	MAX.	TYP.(1)	MAX.	TYP.(1)	MAX.	
t_{WHQV1} t_{EHQV1}	Word/Byte Write Time	32K word Block	2	44.6		17.7		12.6		µS
		4K word Block	2	45.9		26.1		24.5		µS
	Block Write Time	32K word Block	2, 4	1.46		0.58		0.42		S
		4K word Block	2, 4	0.19		0.11		0.11		S
t_{WHQV2} t_{EHQV2}	Block Erase Time	32K word Block	2	1.14		0.61		0.51		S
		4K word Block	2	0.38		0.32		0.31		S
t_{WHRH1} t_{EHRH1}	Word/Byte Write Suspend Latency Time to Read			7	8	6	8	6	7	µS
t_{WHRH2} t_{EHRH2}	Erase Suspend Latency Time to Read			18	22	11	14	11	14	µS

Note: See 5V V_{DD} Block Erase and Word/Byte Write Performance for Notes 1 through 4.

V_{DD} = 3.3V ±0.3V, T_A = 0 ° C to +70° C

SYM.	PARAMETER		NOTE	V_{PP} = 2.7V – 3.6V		V_{PP} = 4.5V – 5.5V		V_{PP} = 11.4V – 12.6V		UNIT
				Typ.(1)	Max.	Typ.(1)	Max.	Typ.(1)	Max.	
t_{WHQV1} t_{EHQV1}	Word/Byte Write Time	32K word Block	2	44		17.3		12.3		µS
		4K word Block	2	45		25.6		24		µS
	Block Write Time	32K word Block	2, 4	1.44		0.57		0.41		S
		4K word Block	2, 4	0.19		0.11		0.1		S
t_{WHQV2} t_{EHQV2}	Block Erase Time	32K word Block	2	1.11		0.59		0.5		S
		4K word Block	2	0.37		0.31		0.3		S
t_{WHRH1} t_{EHRH1}	Word/Byte Write Suspend Latency Time to Read			6	7	5	7	5	6	µS
t_{WHRH2} t_{EHRH2}	Erase Suspend Latency Time to Read			16.2	20	9.6	12	9.6	12	µS

Note: See 5V V_{DD} Block Erase and Word/Byte Write Performance for Notes 1 through 4.

V_{DD} = 5V ±0.5V, 5V ±0.25V, T_A = 0 ° C to +70° C

SYM.	PARAMETER		NOTE	V_{PP} = 4.5V – 5.5V		V_{PP} = 11.4V – 12.6V		UNIT
				Typ.(1)	Max.	Typ.(1)	Max.	
t_{WHQV1} t_{EHQV1}	Word/Byte Write Time	32K word Block	2	12.2		8.4		µS
		4K word Block	2	18.3		17		µS
	Block Write Time	32K word Block	2, 4	0.4		0.28		S
		4K word Block	2, 4	0.08		0.07		S
t_{WHQV2} t_{EHQV2}	Block Erase Time	32K word Block	2	0.46		0.39		S
		4K word Block	2	0.26		0.25		S
t_{WHRH1} t_{EHRH1}	Word/Byte Write Suspend Latency Time to Read			5	6	4	5	µS
t_{WHRH2} t_{EHRH2}	Erase Suspend Latency Time to Read			9.6	12	9.6	12	µS

Notes:

1. Typical values measured at T_A = +25° C and nominal voltages. Subject to change based on device characterization.
2. Excludes system-level overhead.
3. Sampled but not 100% tested.
4. All values are in word mode (#BYTE = V_{IH}). At byte mode (#BYTE = V_{IL}), those values are double.

12. FLASH MEMORY W28V400 FAMILY DATA PROTECTION

Noises having a level exceeding the limit specified in this document may be generated under specific operating conditions on some systems.

Such noises, when induced onto #WE signal or power supply, may be interpreted as false commands, and which will cause undesired memory updating.

To protect the data stored in the flash memory against unwanted overwriting, systems operating with the flash memory should have the following write protect designs, as appropriate:

1. Protecting data in specific block

By setting a #WP to low, only the boot block can be protected against overwriting.
Parameter and main blocks cannot be locked.
System program, etc., can be locked by storing them in the boot block.
When a high voltage is applied to #RESET, overwrite operation is enabled for all blocks.

2. Data protection through V_{PP}

When the level of V_{PP} is lower than V_{PPLK} (lockout voltage), write operation on the flash memory is disabled. All blocks are locked and the data in the blocks are completely write protected.

3. Data protection through #RESET

When the #RESET is kept low during power up and power down sequence such as voltage transition, write operation on the flash memory is disabled, write protecting all blocks.

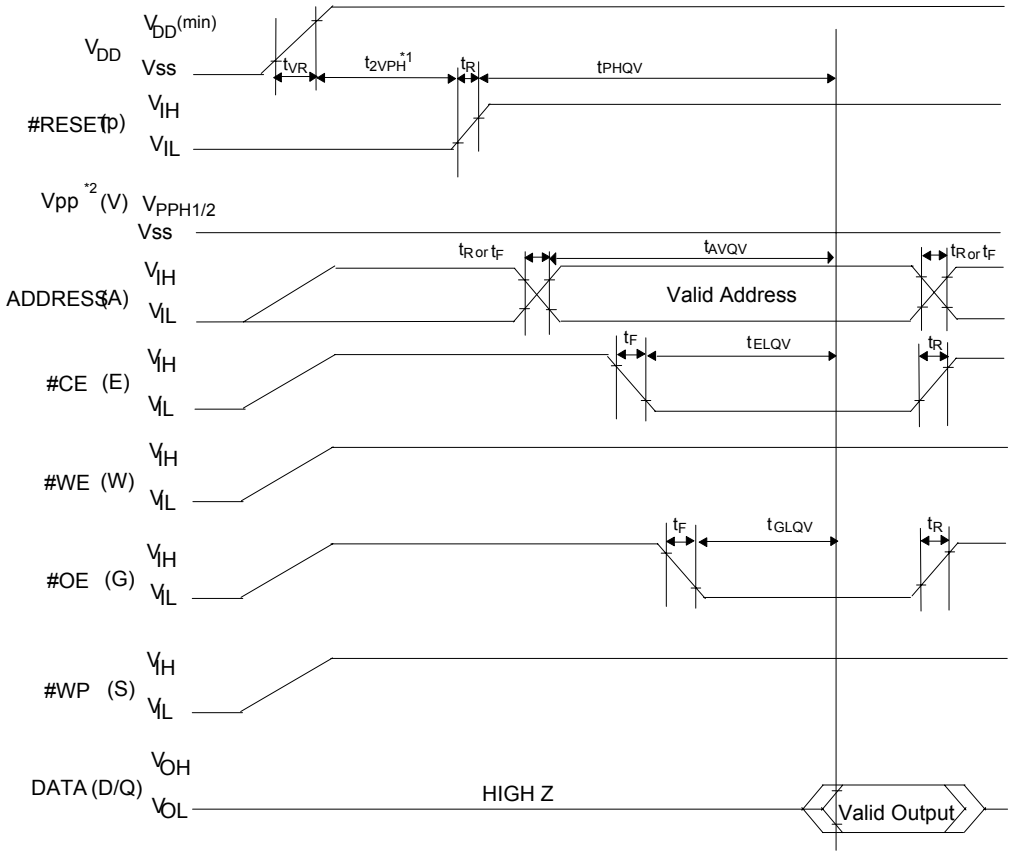
4. Noise rejection of #WE

Consider noise rejection of #WE in order to prevent false write command input.

Recommended Operating Conditions

At Device Power-up

AC timing illustrated in Figure 18 is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.



*1 t_{5VPH} for the device in 5V operations.

*2 To prevent the unwanted writes, system designers should consider the V_{PP} switch, which connects V_{PP} to V_{SS} during read operations and $V_{PPH1/2/3}$ during write or erase operations.

Figure 18. AC Timing at Device Power-up

For the AC specifications t_{VR}, t_R, t_F in the figure, refer to the next page. See the “ELECTRICAL SPECIFICATIONS“ described in specifications for the supply voltage range, the operating temperature and the AC specifications not shown in the next page.

Rise and Fall Time

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
V_{DD} Rise Time (Note 1)	t_{VR}	0.5	30000	μS/ V
Input Signal Rise Time (Note 1, 2)	t_R		1	μS/ V
Input Signal Fall Time (Note 1, 2)	t_F		1	μS/ V

Notes:

1. Sampled, not 100% tested.
2. This specification is applied for not only the device power-up but also the normal operations. t_R (Max.) and t_F (Max.) for #RESET are 100 μS/V

Glitch Noises

Do not input the glitch noises which are below V_{IH} (Min.) or above V_{IL} (Max.) on address, data, reset, and control signals, as shown in Figure 19 (b). The acceptable glitch noises are illustrated in Figure 19 (a).

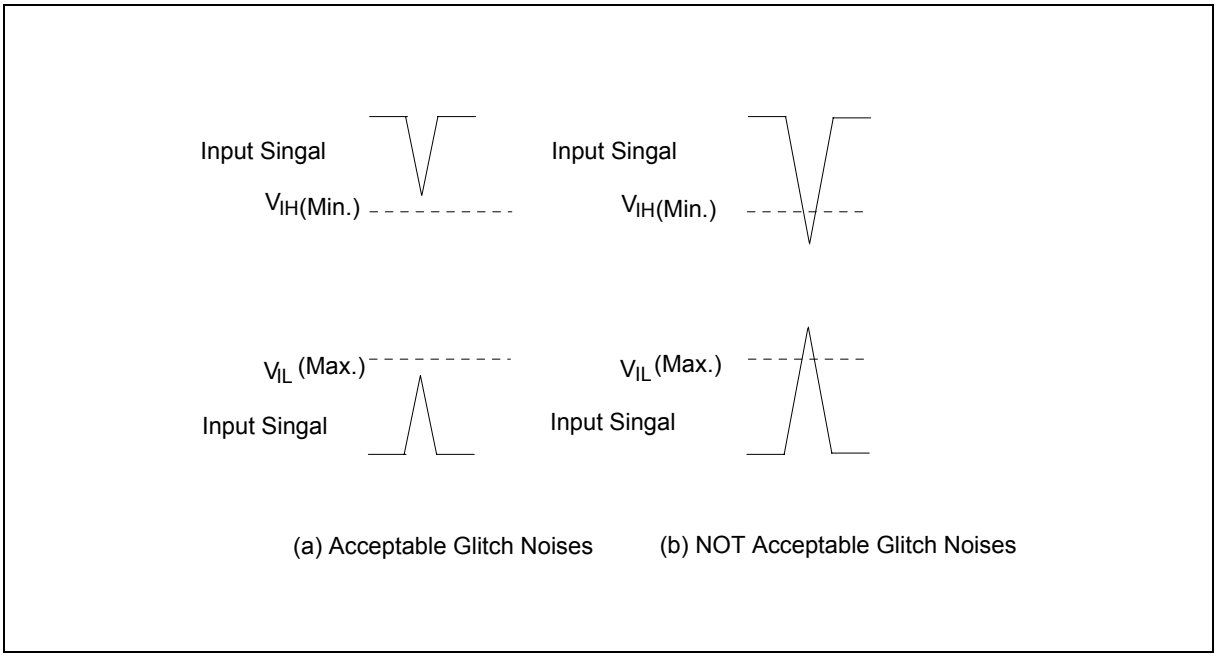


Figure 19. Waveform for Glitch Noises

See the "DC CHARACTERISTICS" described in specifications for V_{IH} (Min.) and V_{IL} (Max.).

13. ORDERING INFORMATION

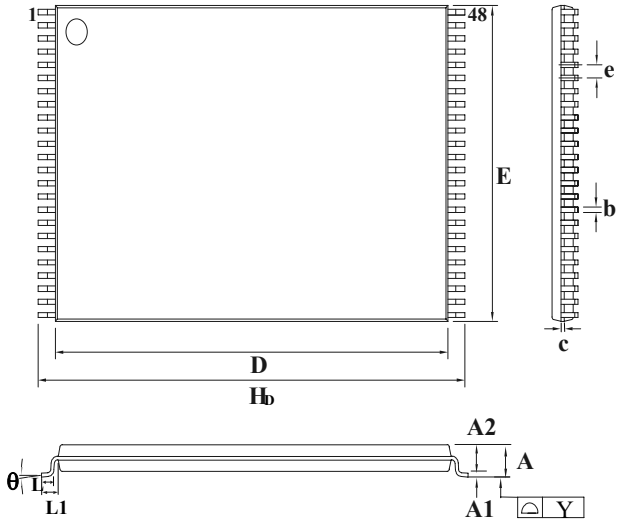
PART NO.	ACCESS TIME (nS)	OPERATING TEMPERATURE (°C)	BOOT BLOCK	PACKAGE
W28V400BT85C	85	0 – 70	Bottom Boot	48L TSOP
W28V400TT85C	85	0 – 70	Top Boot	48L TSOP

Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

14. PACKAGE DIMENSION

48-Lead Standard Thin Small Outline Package (measured in millimeters)



Sym.	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.075	0.125	0.175	0.003	0.005	0.007
A2	0.90	1.00	1.10	0.035	0.039	0.043
D	18.2	18.4	18.6	0.718	0.724	0.730
H_D	19.7	20.0	20.3	0.775	0.787	0.799
E	11.8	12.0	12.2	0.466	0.472	0.478
b	0.12	0.20	0.28	0.005	0.011	0.017
c	0.10	—	0.21	0.004	—	0.008
e	—	0.50	—	—	0.020	—
L	0.35	0.50	0.65	0.020	0.026	0.032
L1	—	0.80	—	—	0.031	—
Y	—	—	0.10	—	—	0.004
θ	0	—	8	0	—	8

15. VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	May 22, 2002	-	Initial Issued
A2	Aug. 5, 2002	All	Update descriptions and correct typo
A3	Nov. 18, 2002	45	Correct the typo in Figure 18
A4	Apr. 11, 2003	All	Update descriptions and correct typo

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